1000Base-X PCS/PMA Controller Core

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Chapter 1

1000BASE-X PCS/PMA DATA SHEET

So-Logic's 1000Base-X PCS core implements 1000Base-X PCS/PMA sublayer from the IEEE Std. 802.3-2008 specification.

It can use any available Xilinx MGT transceivers to implement required physical signaling. For the interface with the MAC layer core uses standard GMII interface.

The so_ip_eth_1000BaseX_pcs_pma core can be evaluated using Xilinx Evaluation Platforms before actual purchase. This is achieved by using a demonstration bit files for KC705 platform that allows the user to connect the So-Logic's complete 1G Ethernet solution system to some other Ethernet enabled device (PC or some Ethernet tester equipment) and evaluate system performance under different transfer scenarios.

1.1 FEATURES

- Fully compliant with the 1000Base-X Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) operation as defined in the EEE Std. 802.3-2008 specification
- Supports 10/100/1000 Mb/s Ethernet communication speeds
- Uses standard GMII interface to connect to the MAC layer
- Integrated transceiver interface using one of the following:
  - Zynq®-7000 All Programmable (AP) SoC GTX Transceiver
  - Kintex-7 FPGA GTX Transceiver
- Low frequency operation
  - IP Core system clock at 125 MHz
- Supports SGMII Auto-Negotiation for communication with the external Physical-Side Interface (PHY) device

1.2 APPLICATIONS

- LAN networking
- Industrial Ethernet
- Distributed Storage Area Networks
- Cloud computing

1.3 DELIVERABLES

- Source code:
  - VHDL Source Code
- VHDL test bench environment
  - Tests with reference responses
- Technical documentation
  - Datasheet
  - Installation notes
  - User manual
- Instantiation templates
- Example application
- Technical Support
  - IP Core implementation support
  - Variable length maintenance
  - Delivery of IP Core updates, minor and major changes
  - Delivery of documentation updates
  - Telephone & email support

1.4 LICENSING

Netlist License

- Post-synthesis netlist
- Self checking testbench
- Test vectors for testing the core
- Place&Route scripts
- Constraints
- Instantiation template
- Documentation

VHDL Source License

- VHDL RTL source code
- Complete verification plan together with the functional verification environment to verify the correct operation of the core
- Self checking test bench
- Vectors for testing the functionality of the core
- Simulation & synthesis scripts
- Documentation

1.5 SYMBOL

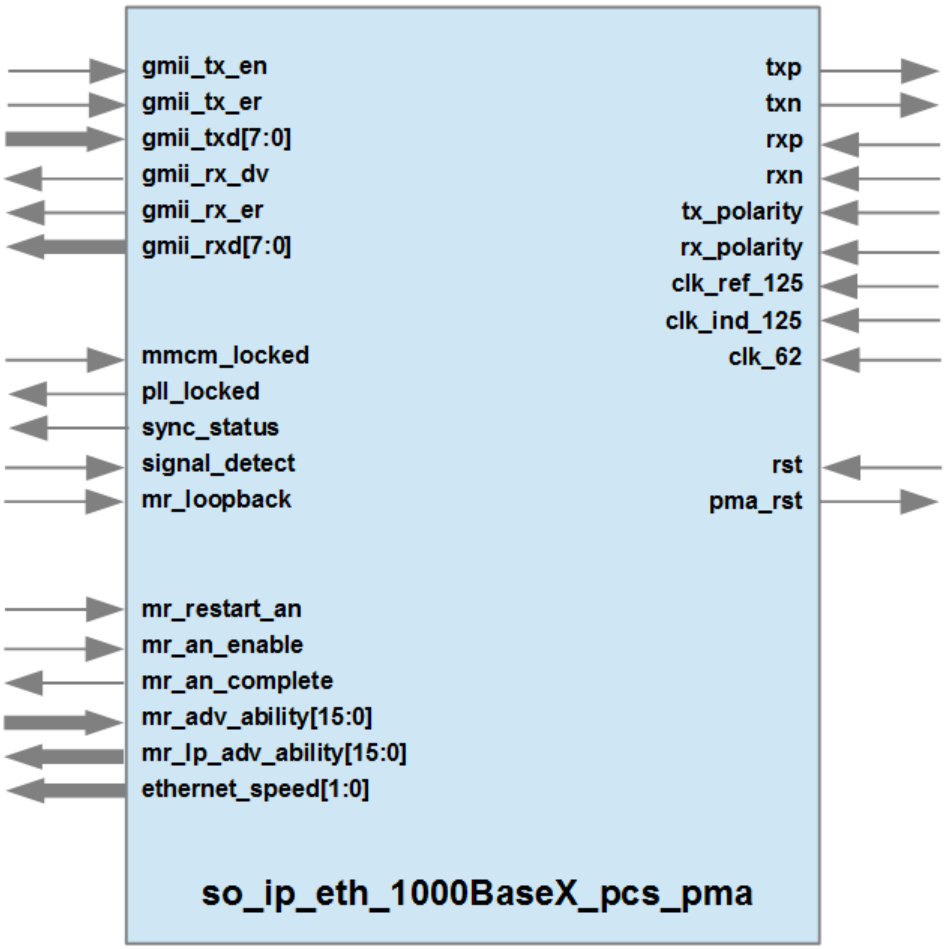

Figure 1.1: Symbol

1.6 PIN DESCRIPTION

Name	Signal Direction	Description
GMII Interface		
gmii_tx en	Input	GMII transmit enable input signal
gmii_tx er	Input	GMII transmit error input signal
gmii_txd[7:0]	Input	GMII transmit data input signal
gmii_rx dv	Output	GMII receive data valid output signal
gmii_rx er	Output	GMII receive error output signal
gmii_rxd[7:0]	Output	GMII receive data signal
Status Signal and Misc. Ports		
mmcm_locked	Input	Informs the PCS core that the *clk_125* is stable
pll_locked	Output	Indication that the GTX Transceiver CPLL has locked
sync_status	Output	Indication that the PCS core has established the link PCS

signal_detect	Input	A signal used to reset the PCS core Synchronization block. If the optical module is used as a PCS core peer, this signal should be connected to the module's indication of the presence of light, where value of 1 indicates the detectable presence of light, and 0 indicates some kind of fault. This signal can also be used by higher Ethernet layers to restart the synchronization process.
mr_loopback	Input	When set to 1, the signal resets the PCS core Synchronization block and indicates to it that the data is being looped back through the PHY
Auto-Negotiation Interface		
mr_restart_an	Input	Restarts the Auto-Negotiation process
mr_an_enable	Input	When high enables the auto-negotiation process
mr_an_complete	Output	Signals that auto-negotiation has completed successfully
mr_adv_ability[15:0]	Input	For SGMII auto-negotiation advertisement ability is hardwired to the value 0x4001
mr_lp_adv_ability[15:0]	Output	Holds the link partner ability after auto-negotiation has completed
ethernet_speed[1:0]	Output	Indicates which speed should be used for MAC clocking: 00 - 10Mbps (1.25MHz), 01 - 100Mbps (12.5MHz), 10 - 1Gbps (125MHz), 11 - reserved
MGT Interface		
txp	Output	MGT positive TX output
txn	Output	MGT negative TX output
rxp	Input	MGT positive RX input
rxn	Input	MGT negative RX input
tx_polarity	Input	MGT port used to invert the polarity of outgoing data
rx_polarity	Input	MGT port used to invert the polarity of incoming data
clk_ref_125	Input	125 MHz reference clock from transceiver's IBUFDS
clk_ind_125	Input	125 MHz clock, independent from the *clk_ref_125* used for GTX Transceiver reset FSMs and startup
clk_62	Input	62.5 MHz clock, independent from the *clk_ref_125* used for GTX Transceiver reset FSMs and startup
Reset Interface		
rst	Input	Reset signal for the PCS core logic only
pma rst	Input	Reset signal for the GTX Transceiver

1.7 BLOCK DIAGRAM

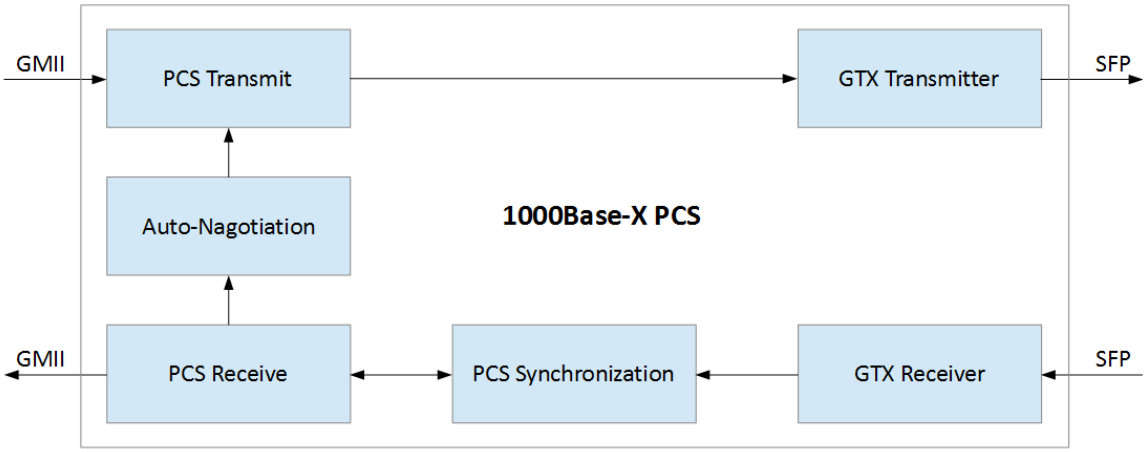

Figure 1.2: Block Diagram

1.8 FUNCTIONAL DESCRIPTION

The 1000Base-X PCS Core together with the board specific GTX transceivers implements the Physical Coding Sub-layer and the Physical Medium Attachment Sub-layer. This core implements the following functionality:

- GMII data stream encapsulation and encoding
- Synchronization and decoding of received data
- Ethernet speed and option adaptation using Auto-negotiation

Top level block diagram of the 1000Base-X PCS Core is shown in the picture above. The PCS core consists of the following modules:

- PCS Transmit
- PCS Receive
- PCS Synchronization
- Auto-Negotiation

PCS Transmit

The PCS Transmit process receives data from the MAC layer, encodes 8bit data bytes into 10bit code-groups and sends those to the physical sublayer.

The PCS Transmit plays the following roles in the 1G Ethernet transmission process:

- Encodes the data per 8B/10B encoding scheme
- Generates the running disparity. Running disparity is employed in the 1G Ethernet to balance the DC value on the line, by balancing the number of ones and zeros transmitted
- Adds PCS headers and footers from the GMII protocol data stream
- Sends the Auto-Negotiation configuration value during the Auto-Negotiation process

PCS Receive

The PCS Receive process continuously receives the code-groups from the physical sublayer. The PCS Receive process monitors these code-groups and generates the GMII signals.

The PCS Receive plays the following roles in the 1G Ethernet reception process:

- Makes sure that it is synchronized to the data transmitter and rejects data if it is out of sync
- Identifies the start and the end of the MAC frame in the data being received
- Decodes the data per 8B/10B decoding scheme. This scheme is used in the 1G Ethernet to ensure a good number of transitions on the transmission line for the clock recovery
- Takes care of the running disparity. Running disparity is employed in 1G Ethernet to balance the DC on the line, by balancing the number of ones and zeros transmitted
- Strips the PCS headers and footers and forms the GMII protocol data stream
- Stores the Auto-Negotiation configuration registers during the Auto-Negotiation process

PSC Synchronization

The PCS Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PCS layer to suspend normal actions.

PSC Synchronization

The Auto-negotiation core controls the PCS transmit and receive behavior.

1.9 VERIFICATION METHODS

1000Base-X PCS core was tested both using sophisticated verification environment and in dedicated hardware platform. Verification environment, together with the developed verification plan, was used to extensively verify the 1000Base-X PCS core operation is in accordance with the IEEE Std. 802.3-2008 specification. After reaching all verification goals, IP core was tested using dedicated hardware platforms, namely Xilinx's KC-705 Evaluation Platform. Using these platforms 1000-Base-X PCS core was implemented in FPGA and connected to various Ethernet-enabled devices to test its operation in a real application and to estimate the performance of the core. The details about the verification methodology that was used and performance results during hardware testing can be obtained from So-Logic upon request.

1.10 DEVICE UTILIZATION & PERFORMANCE

Supported Family	Device	Slices	Slice LUTs	Slice FFs	IOs	BRAMs	MGTs
Kintex-7	XC7K325T-2	222	433	270	379	0	1
Zynq	XC7Z045-2	222	433	270	379	0	1

Notes:

1. All core I/O signals are routed off chip
2. Results were obtained using Xilinx Vivado Design Suite 2014.3 software
3. The synthesis results provided are for reference only. Please contact So-Logic for estimates for your particular application.

1.11 CONTACT INFORMATION

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1.12 REVISION HISTORY

The following table shows the revision history for this document.

Date	Version	Revision
01/11/14	1.0	Initial release.