10GBase-R PCS/PMA Controller Core

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Chapter 1

10GBASE-R PCS/PMA DATA SHEET

So-Logic's 10GBase-R PCS/PMA core implements 1000Base-X PCS/PMA sublayer from the IEEE Std. 802.3-2008 specification.

It can use any available Xilinx MGT transceivers to implement required physical signaling. For the interface with the MAC layer core uses standard XGMII-SDR interface.

The so_ip_eth_10GBaseR_pcs_pma core can be evaluated using Xilinx Evaluation Platforms before actual purchase. This is achieved by using a demonstration bit files for KC705 platform that allows the user to connect the So-Logic's complete 10G Ethernet solution system to some other Ethernet enabled device (PC or some Ethernet tester equipment) and evaluate system performance under different transfer scenarios.

1.1 FEATURES

- Fully compliant with the IEEE Std. 802.3-2008 specification
- AXI4-Stream user side interface for transmission and reception of Ethernet frames
- Supports XGMII-SDR as well as providing connectivity to So-Logic's 10GBase-R PCS/PMA core
- Low frequency operation
  - IP Core system clocks at 156.25 MHz for 10 Gb/s data rates
- Configuration and monitoring through an AXI4-Lite interface
- MAC flow control pause frame support
- Statistic counters
- Configurable interframe gap
- Automatic padding and FCS calculation
- Configurable support for the jumbo frames
- Configurable maximum frame length check
- Configurable receive address filter

1.2 APPLICATIONS

- LAN networking
- Industrial Ethernet
- Distributed Storage Area Networks
- Cloud computing

1.3 DELIVERABLES

- Source code:
  - VHDL Source Code
- VHDL test bench environment
  - Tests with reference responses
- Technical documentation
  - Datasheet
  - Installation notes
  - User manual
- Instantiation templates
- Example application
- Technical Support
  - IP Core implementation support
  - Variable length maintenance
  - Delivery of IP Core updates, minor and major changes
  - Delivery of documentation updates
  - Telephone & email support

1.4 LICENSING

Netlist License

- Post-synthesis netlist
- Self checking testbench
- Test vectors for testing the core
- Place&Route scripts
- Constraints
- Instantiation template
- Documentation

VHDL Source License

- VHDL RTL source code
- Complete verification plan together with test benches needed to verify correct operation of the core
- Self checking test bench
- Vectors for testing the functionality of the core
- Simulation & synthesis scripts
- Documentation

1.5 SYMBOL

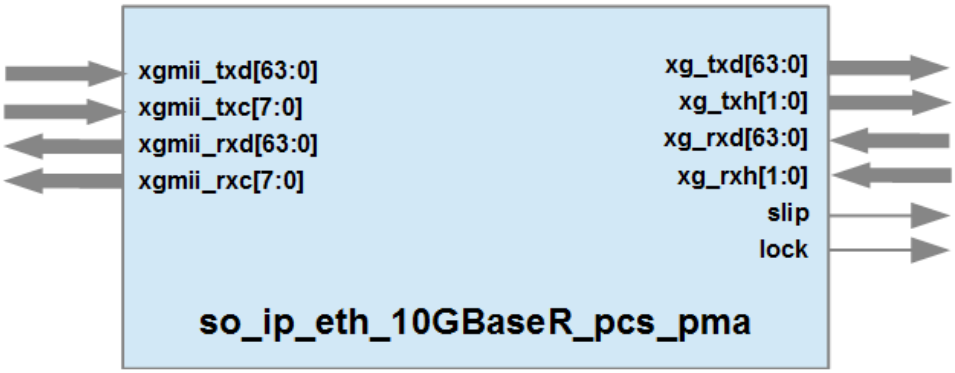

Figure 1.1: Symbol

1.6 PIN DESCRIPTION

Name	Signal Direction	Description
XGMII-SDR Interface		
xgmii_txd[63:0]	Output	XGMII TX data output
xgmii_txc[7:0]	Output	XGMII TX control output
xgmii_rxd[63:0]	Input	XGMII RX data input
xgmii_rxc[7:0]	Input	XGMII RX control input
10GBase-R to SerDes Interface		
xg_txd[63:0]	Output	64 bit output data
xg_txh[1:0]	Output	2 bit output header for synchronization
xg_rxd[63:0]	Input	64 bit input data
xg_rxh[1:0]	Input	2 bit input header for synchronization
slip	Output	Slip signal for 10G gearbox inside SerDes(GTX)
lock	Output	Lock signal for the 10GBase-R core

1.7 BLOCK DIAGRAM

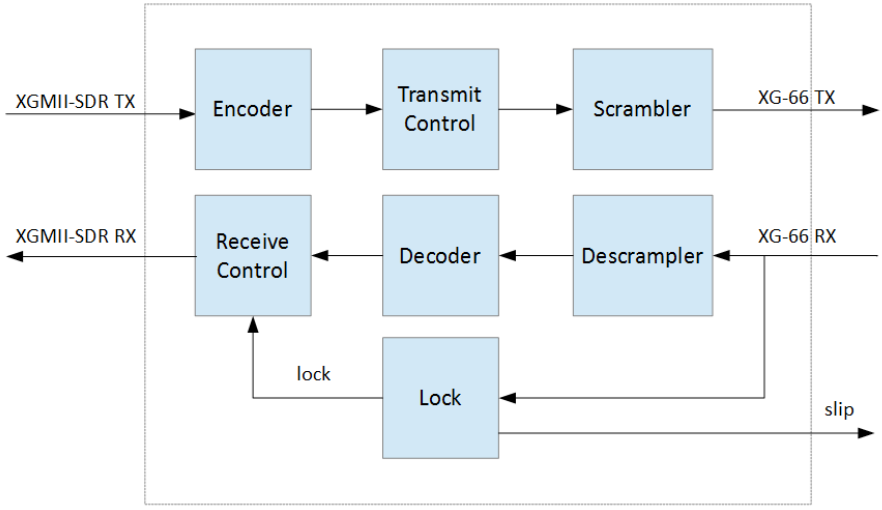

Figure 1.2: Block Diagram

1.8 FUNCTIONAL DESCRIPTION

The 10GBase-R Core together with the board specific GTX transceivers implements the Physical Coding Sub-layer and the Physical Medium Attachment Sub-layer. This core implements the following functionality:

- XGMII-SDR data stream encapsulation and encoding
- Synchronization and decoding of received data
- Scrambling and unscrambling of data stream

The 10GBase-R core has several sub-modules. Each of the modules implements one part of 10GBase-R specification. The modules are :

- Encoder
- Transmit control
- Scrambler
- Descrambler
- Decoder
- Receive control
- Lock

Encoder

The “Encoder” component of the XPCS-TX is implemented in the files “xpcs_encoder6466_rtl.vhd”, “xpcs_encoder6466_control_convertor_rtl.vhd”, and “xpcs_defs_pkg.vhd”. It implements the coding part of the section 49.2.4 of the “IEEE Std 802.3-2008”. For more details about symbol meaning and detailed description of coding system, read the IEEE section.

The “Encoder” recognize the XGMII control block format shown in figure 49-7 of the “IEEE Std 802.3-2008” (Error: Reference source not found). The module inserts the block type field according to XGMII control block format. This is implemented in the file “xpcs_encoder6466_rtl.vhd”.

The control character conversion is done in the file “xpcs_encoder6466_control_convertor_rtl.vhd”. It is combinatorial circuit. The conversion of symbols is given in the table 49-1 of the “IEEE Std 802.3-2008”.

The definitions of all needed symbols are in the file “xpcs_defs_pkg.vhd”. All XGMII symbols, block format types and control codes are defined in this file.

Transmit Control

The “Transmit Control” component of XPCS-TX is implemented in the file “xpcs_transmit_rtl.vhd”. It implements the section 49.2.5 of the “IEEE Std 802.3-2008”. The module is implemented as FSM equivalent to the figure 49-14 of the “IEEE Std 802.3-2008” and this figure is detailed description how of the unit works.

The purpose of this transmit control is to ensure that the data forms a frame. If some random data is received that does not forms a frame than error codes will be inserted in the data stream.

Scrambler

The “Scrambler” component of the XPCS-TX is implemented in the file “xpcs_scrambler_rtl.vhd”. It implements the section 49.2.6 of the “IEEE Std 802.3-2008”. The serial scrambler diagram is shown in the figure 49-8 of the “IEEE Std 802.3-2008”. This module implements scrambling in parallel, so all job is done in one cycle.

Descrambler

The “Descrambler” component of the XPCS-RX is implemented in the file “xpcs_descrambler_rtl.vhd”. It implements the section 49.2.10 of the “IEEE Std 802.3-2008”. The serial unscrambler diagram is shown in the figure 49-10 of the “IEEE Std 802.3-2008”. This module implements unscrambling in parallel, so all job is done in one cycle.

Decoder

The “Decoder” component of the XPCS-RX is implemented in the files “xpcs_decoder6466_rtl.vhd”, “xpcs_decoder6466_control_convertor_rtl.vhd”, and “xpcs_defs_pkg.vhd”. It implements the decoding part of the section 49.2.4 of the “IEEE Std 802.3-2008”. For more details about symbol meaning and detailed description of coding system, read the IEEE section.

The decoder recognize the block payload types shown in figure 49-7 of the “IEEE Std 802.3- 2008”. This is implemented in the file “xpcs_decoder6466_rtl.vhd”. By means of the type the module knows where to expects control characters.

The control character conversion is done in the file “xpcs_decoder6466_control_convertor_rtl.vhd”. It is combinatorial circuit. The conversion of symbols is given in the table 49-1 of the “IEEE Std 802.3-2008”.

The definitions of all needed symbols are in the file “xpcs_defs_pkg.vhd”. All XGMII symbols, block format types and control codes are defined in this file.

Receive Control

The “Receive Control” component of XPCS-RX is implemented in the file “xpcs_receive_rtl.vhd”. It implements the section 49.2.11 of the “IEEE Std 802.3-2008”. The module is implemented as FSM equivalent to the figure 49-15 of the “IEEE Std 802.3-2008” and this figure is detailed description how of the unit works.

The purpose of this receive control is to ensure that the data forms a frame. If some random data is received that does not forms a frame than error codes will be inserted in the data stream.

Lock

The “Lock” component of XPCS-RX is implemented in the file “xpcs_lock_rtl.vhd”. It implements the section 49.2.9 of the “IEEE Std 802.3-2008”.

This module synchronizes to a data transmitter. In brief, the module try to find where in the received data stream, is always a transition between two successive bits. According to the 64/66 coding system, there is 66 possible places where the transition can occur. In the one position there is always the transition and that is the synchronization point.

1.9 VERIFICATION METHODS

10GBase-R PCS/PMA core was tested both using sophisticated verification environment and in dedicated hardware platform. Verification environment, together with the developed verification plan, was used to extensively verify the 10GBase-R PCS/PMA core operation is in accordance with the IEEE Std. 802.3-2008 specification. After reaching all verification goals, IP core was tested using dedicated hardware platforms, namely Xilinx’s KC-705 Evaluation Platform. Using these platforms 10GBase-R PCS/PMA core was implemented in FPGA and connected to various Ethernet-enabled devices to test its operation in a real application and to estimate the performance of the core. The details about the verification methodology that was used and performance results during hardware testing can be obtained from So-Logic upon request.

1.10 DEVICE UTILIZATION & PERFORMANCE

Supported Family	Device	Slices	Slice LUTs	Slice FFs	IOs	BRAMs	MGTs
Kintex-7	XC7K325T-2	309	742	641	379	0	1
Zynq	XC7Z045-2	309	742	641	379	0	1

Notes:

1. All core I/O signals are routed off chip
2. Results were obtained using Xilinx Vivado Design Suite 2014.3 software
3. The synthesis results provided are for reference only. Please contact So-Logic for estimates for your particular application.

1.11 CONTACT INFORMATION

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1.12 REVISION HISTORY

The following table shows the revision history for this document.

Date	Version	Revision
01/11/14	1.0	Initial release.