10G Ethernet MAC Controller Core

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Chapter 1

10G ETHERNET MAC DATA SHEET

So-Logic's 10G Ethernet MAC core implements MAC sublayer from the IEEE Std. 802.3-2008 specification.

For the interface with the Host processor IP core uses standard AXI4-Stream interface for data transfers and AXI4-Lite interface for the configuration, and for the interface with the PCS layer standard XGMII-SDR interface.

The so_ip_eth_10G_mac core can be evaluated using Xilinx Evaluation Platforms before actual purchase. This is achieved by using a demonstration bit files for KC705 platform that allows the user to connect the So-Logic's complete 10G Ethernet solution system to some other Ethernet enabled device (PC or some Ethernet tester equipment) and evaluate system performance under different transfer scenarios.

1.1 FEATURES

- Fully compliant with the IEEE Std. 802.3-2008 specification
- AXI4-Stream user side interface for transmission and reception of Ethernet frames
- Supports XGMII-SDR as well as providing connectivity to So-Logic's 10GBase-R PCS/PMA core
- Low frequency operation
  - IP Core system clocks at 156.25 MHz for 10 Gb/s data rates
- Configuration and monitoring through an AXI4-Lite interface
- MAC flow control pause frame support
- Statistic counters
- Configurable interframe gap
- Automatic padding and FCS calculation
- Configurable support for the jumbo frames
- Configurable maximum frame length check
- Configurable receive address filter

1.2 APPLICATIONS

- LAN networking
- Industrial Ethernet
- Distributed Storage Area Networks
- Cloud computing

1.3 DELIVERABLES

- Source code:
  - VHDL Source Code
- VHDL test bench environment
  - Tests with reference responses
- Technical documentation
  - Datasheet
  - Installation notes
  - User manual
- Instantiation templates
- Example application
- Technical Support
  - IP Core implementation support
  - Variable length maintenance
  - Delivery of IP Core updates, minor and major changes
  - Delivery of documentation updates
  - Telephone & email support

1.4 LICENSING

Netlist License

- Post-synthesis netlist
- Self checking testbench
- Test vectors for testing the core
- Place&Route scripts
- Constraints
- Instantiation template
- Documentation

VHDL Source License

- VHDL RTL source code
- Complete verification plan together with test benches needed to verify correct operation of the core
- Self checking test bench
- Vectors for testing the functionality of the core
- Simulation & synthesis scripts
- Documentation

1.5 SYMBOL

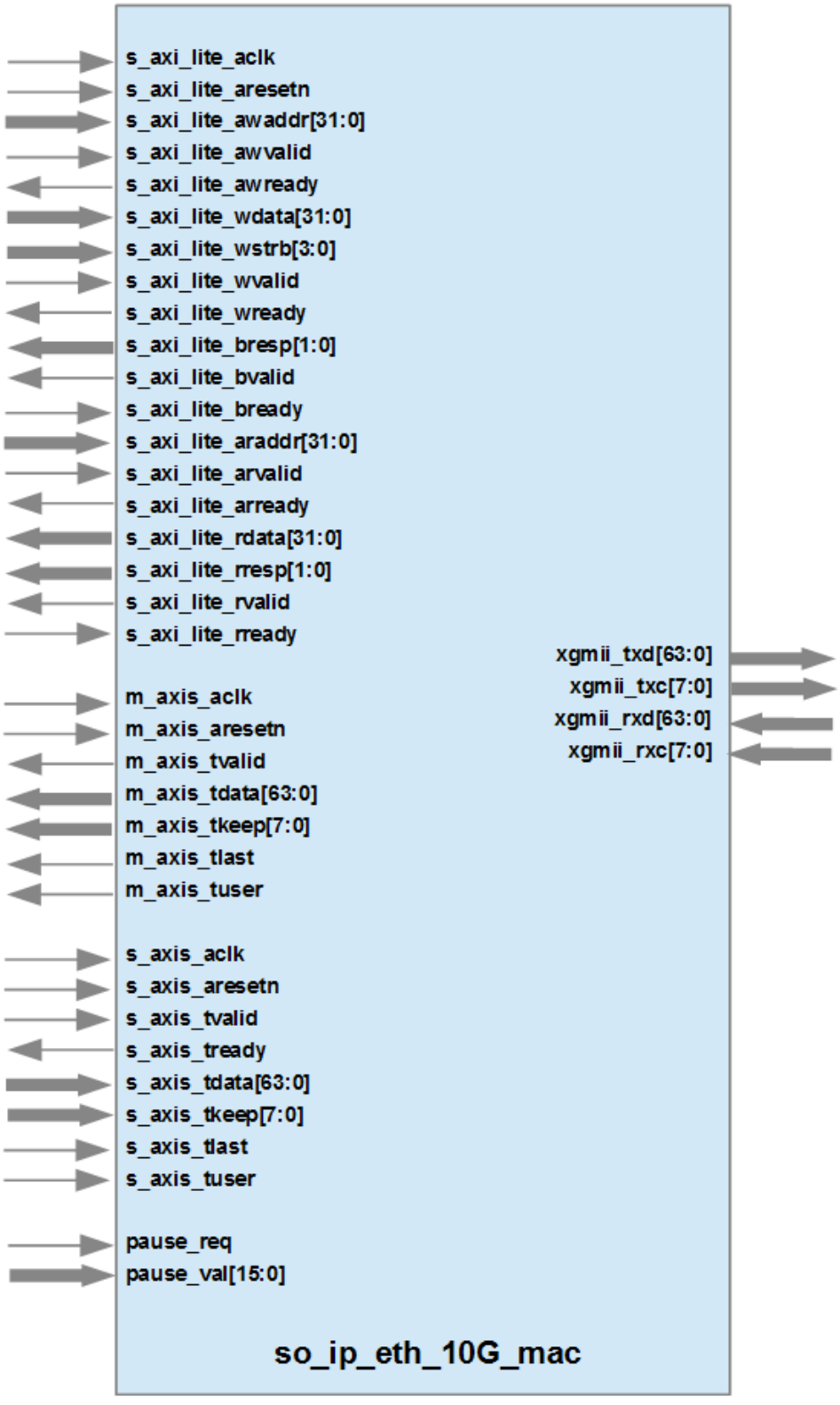

Figure 1.1: Symbol

1.6 PIN DESCRIPTION

Name	Signal Direction	Description
AXI4 Lite Interface		
s_axi_lite_aclk	Input	Clock for AXI4-Lite
s_axi_lite_aresetn	Input	Local reset for AXI4-Lite interface
s_axi_lite_awaddr[31:0]	Input	Write Address
s_axi_lite_awvalid	Input	Write Address valid
s_axi_lite_awready	Output	Write Address ready
s_axi_lite_wdata[31:0]	Input	Write Data
s_axi_lite_wstrb[3:0]	Input	Unused
s_axi_lite_wvalid	Input	Write Data valid
s_axi_lite_wready	Output	Write Data ready
s_axi_lite_bresp[1:0]	Output	Write Response
s_axi_lite_bvalid	Output	Write Response valid
s_axi_lite_bready	Input	Write Response ready
s_axi_lite_araddr[31:0]	Input	Read Address
s_axi_lite_arvalid	Input	Read Address valid
s_axi_lite_arready	Output	Read Address ready
s_axi_lite_rdata[31:0]	Output	Read Data
s_axi_lite_rresp[1:0]	Output	Read Response
s_axi_lite_rvalid	Output	Read Data/Response valid
s_axi_lite_rready	Input	Read Data/Response ready
AXI4 Stream Receive Interface		
m_axis_aclk	Input	Clock to which all AXI4 Receive signals are synchronous
m_axis_aresetn	Input	Reset signal for the AXI4 Receive interface
m_axis_tvalid	Output	Indicates that **m_axis_tdata** contains valid frame data
m_axis_tdata[63:0]	Output	Frame data, split into 8 lanes
m_axis_tkeep[7:0]	Output	Indicate which lanes of the **m_axis_tdata** are carrying valid data. Other lanes should be ignored.
m_axis_tlast	Output	Indicates that the last 64b word of frame data is sent to the user
m_axis_tuser	Output	When asserted together with **m_axis_tlast**, this signal indicates that the received frame should be ignored because it has been identified that it contains errors
AXI4 Stream Transmit Interface		
s_axis_aclk	Input	Clock to which all AXI4 Transmit signals are synchronous
s_axis_aresetn	Input	Reset signal for the AXI4 Transmit interface
s_axis_tvalid	Input	Indicates that **s_axis_tdata** contains valid frame data. Should be at '1' all the time during the frame transmission.

s_axis_tready	Output	Indicates that the core has read current data and that new data need to be supplied
s_axis_tdata[63:0]	Input	Frame data, split into 8 lanes
s_axis_tkeep[7:0]	Input	Indicate which lanes of the **s_axis_tdata** contain valid data. Other lanes should be ignored
s_axis_tlast	Input	Indicates that the last 64b word of data is transmit to the core
s_axis_tuser	Input	When asserted during frame transmission user indicates that the frame should be dropped (the core will flag that the frame contains error)
XGMII-SDR Interface		
xgmii_txd[63:0]	Output	XGMII TX data output
xgmii_txc[7:0]	Output	XGMII TX control output
xgmii_rxd[63:0]	Input	XGMII RX data input
xgmii_rxc[7:0]	Input	XGMII RX control input
Pause Interface		
pause_req	Input	Pause request input port
pause_val[15:0]	Input	Duration of the requested pause, measured in time quanta that last for 512 bits

1.7 BLOCK DIAGRAM

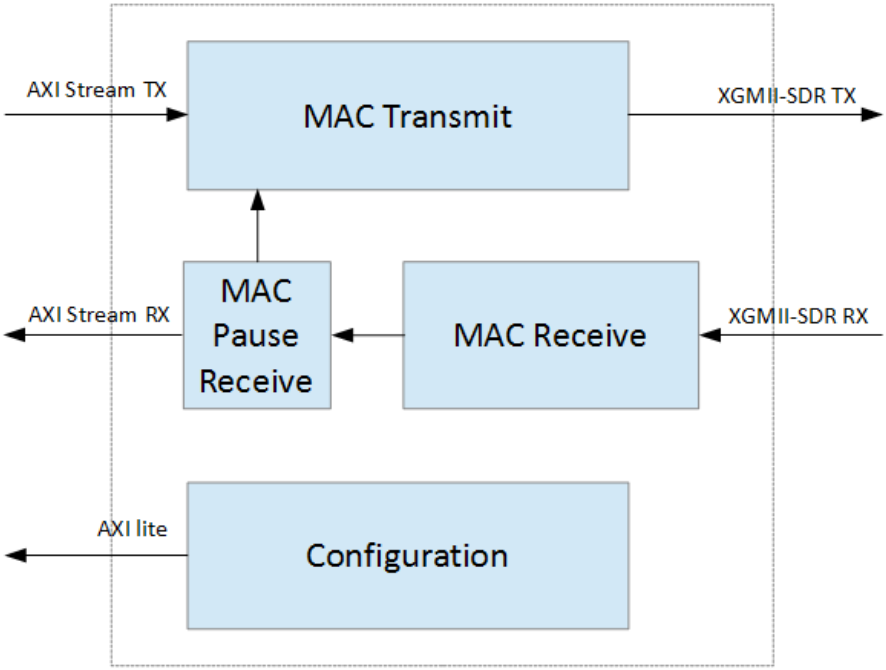

Figure 1.2: Block Diagram

1.8 FUNCTIONAL DESCRIPTION

The 10G Ethernet MAC (XMAC) core has several parts. The MAC transmit receives the frames from the user logic through the AXI Stream transmit interface and sends the result frames to the XGMII-SDR transmit interface. The MAC receive module receives the frames form the lower layers through the XGMII-SDR receive interface. The received frame is then sent to the MAC pause receive. This module checks if the frame is of the pause control type. If not the frame is passed to

the output AXI RX stream. If yes, the MAC transmit is paused for the requested period of time. The configuration module enables the user logic to configure and monitor internal working of the MAC core. The user logic communicates with the configuration module through the AXI Lite interface.

The previous diagram shows all major modules of the so_ip_eth_10G_mac core that is described here in more detail.

MAC Receive

10G MAC Controller MAC Receive is responsible for the frame reception which includes:

1. Frame boundary recognition
2. Recognition of collision fragments
3. Address recognition and frame filtering
4. Error checking
5. Frame disassembly
6. User data output using AXI4 8b Stream protocol
7. Tracking statistics

MAC Transmit

10G MAC Controller MAC Transmit (XMACT) module takes a user supplied frame from the AXI bus and transmits the data to the XGMII-SDR output. The XMACT includes following responsibilities:

1. Add the preamble to the user frame
2. Add SFD (Start Frame Delimiter) to the user frame
3. Add FCS to the user frame
4. Check the length of the input frame
5. Makes an inter-frame gap between frames
6. Track statistic of the transmitted frames

Flow Control

10G Ethernet Flow Control has two functions:

1. Generates pause frames from a dedicated interface
2. Recognizes the pause frames and responds to them

MAC Pause Receive

10G MAC Controller core has two input ports for the pause requests. The user logic can request the pause frame generation with the ports *“pause_req”* and *“pause_val”*. That can be done with asserting the *“pause_req”* signal. The input *“pause_val”* determine how long the pause should last in quanta that lasts 512 bits. For example, if *“pause_val”* is equal to 5 than pause should last for 2560 bits.

1.9 VERIFICATION METHODS

10G MAC controller core was tested both using sophisticated verification environment and in dedicated hardware platform. Verification environment, together with the developed verification plan, was used to extensively verify the 10G MAC controller core operation is in accordance with the IEEE Std. 802.3-2008 specification. After reaching all verification goals, IP core was tested using dedicated hardware platforms, namely Xilinx’s KC-705 Evaluation Platform. Using these platforms 10G MAC controller core was implemented in FPGA and connected to various Ethernet-enabled devices to test its operation in a real application and to estimate the performance of the core. The details about the verification methodology that was used and performance results during hardware testing can be obtained from So-Logic upon request.

1.10 DEVICE UTILIZATION & PERFORMANCE

Supported Family	Device	Slices	Slice LUTs	Slice FFs	IOs	BRAMs	MGTs
Kintex-7	XC7K325T-2	2389	4756	4727	379	0	0
Zynq	XC7Z045-2	2389	4756	4727	379	0	0

Notes:

1. All core I/O signals are routed off chip
2. Results were obtained using Xilinx Vivado Design Suite 2014.3 software
3. The synthesis results provided are for reference only. Please contact So-Logic for estimates for your particular application.

1.11 CONTACT INFORMATION

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1.12 REVISION HISTORY

The following table shows the revision history for this document.

Date	Version	Revision
01/11/14	1.0	Initial release.