so_ip_8051C256

Product Specification

8-bit Microcontroller Core

General Description

The so_ip_8051C256 is a soft core of a 8-bit CPU dedicated for operation with *fast* (on-chip) and *slow* (off-chip) memories.

So_ip_8051C256 soft core is 100% binary compatible with the CPU from industry standard 8051 microcontroller. It executes all ASM51 instructions and has the same instruction set as the 8031. The so_ip_8051C256 serves both software and hardware interrupts.

So_ip_8051C256 has an advanced architecture that enables it to be 4.51 times faster than the CPU from original 8051 microcontroller.

So_ip_8051C256 is delivered with fully automated testbench and a compete set of tests allowing easy package validation at each stage of SoC design flow.

The so_ip_8051C256 is a microcode-free design developed for reuse in FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset.

CPU Features

- 100% software compatible with industry standard 8051
- Advanced architecture enables to execute instructions on average 4.51 times faster compared to original 8051
- 8 times faster multiplication
- 8 times faster division
- 4 times faster addition
- 256 bytes of internal (on-chip) Data Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Program Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Data Memory
- De-multiplexed Address/Data bus to allow easy connection to memory
- Fully synthesizable synchronous design with positive edge clocking and no internal tri-states

Peripherals

- Interrupt Controller
  - 2 priority levels
  - 2 external sources
- Four 8-bit I/O Ports
  - Separate input and output lines

Applications

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Deliverables

- Source code:
  - VHDL Source Code
- VHDL test bench environment
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Instantiation templates
- Example application
- Technical Support
  - IP Core implementation support
  - Variable length maintenance
    - Delivery of IP Core updates, minor and major changes
    - Delivery of documentation updates
    - Telephone & email support

Licensing

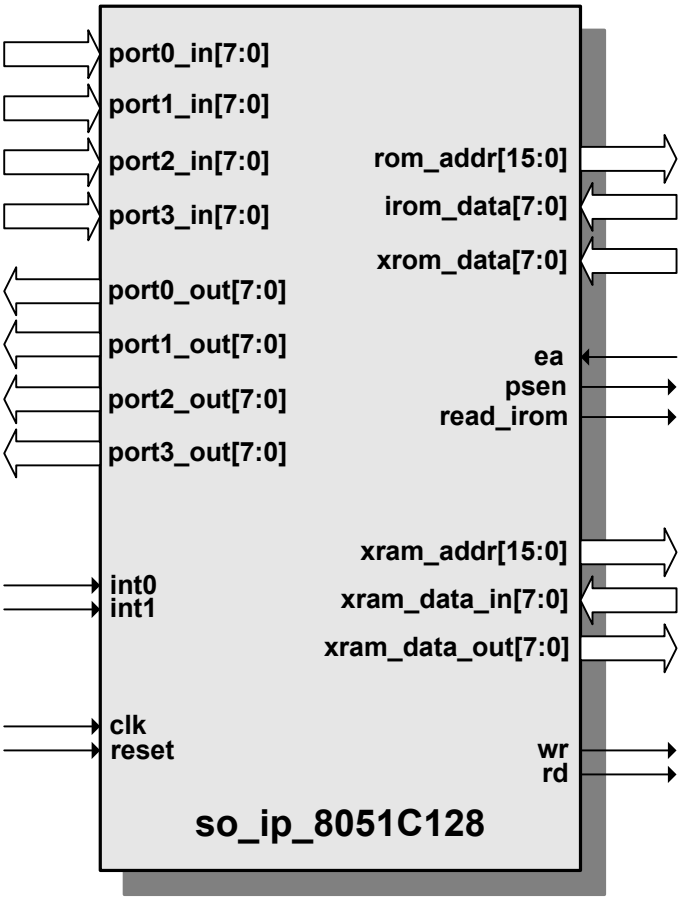
Netlist License

- Post-synthesis netlist
- Self checking testbench
- Test vectors for testing the core
- Place&Route scripts
- Constraints
- Instantiation templates
- Documentation

VHDL Source License

- VHDL RTL source code
- Complete verification plan together with testbenches needed to verify correct operation of the core
- Self checking testbench
- Vectors for testing the functionality of the core
- Simulation & synthesis scripts
- Documentation

Symbol

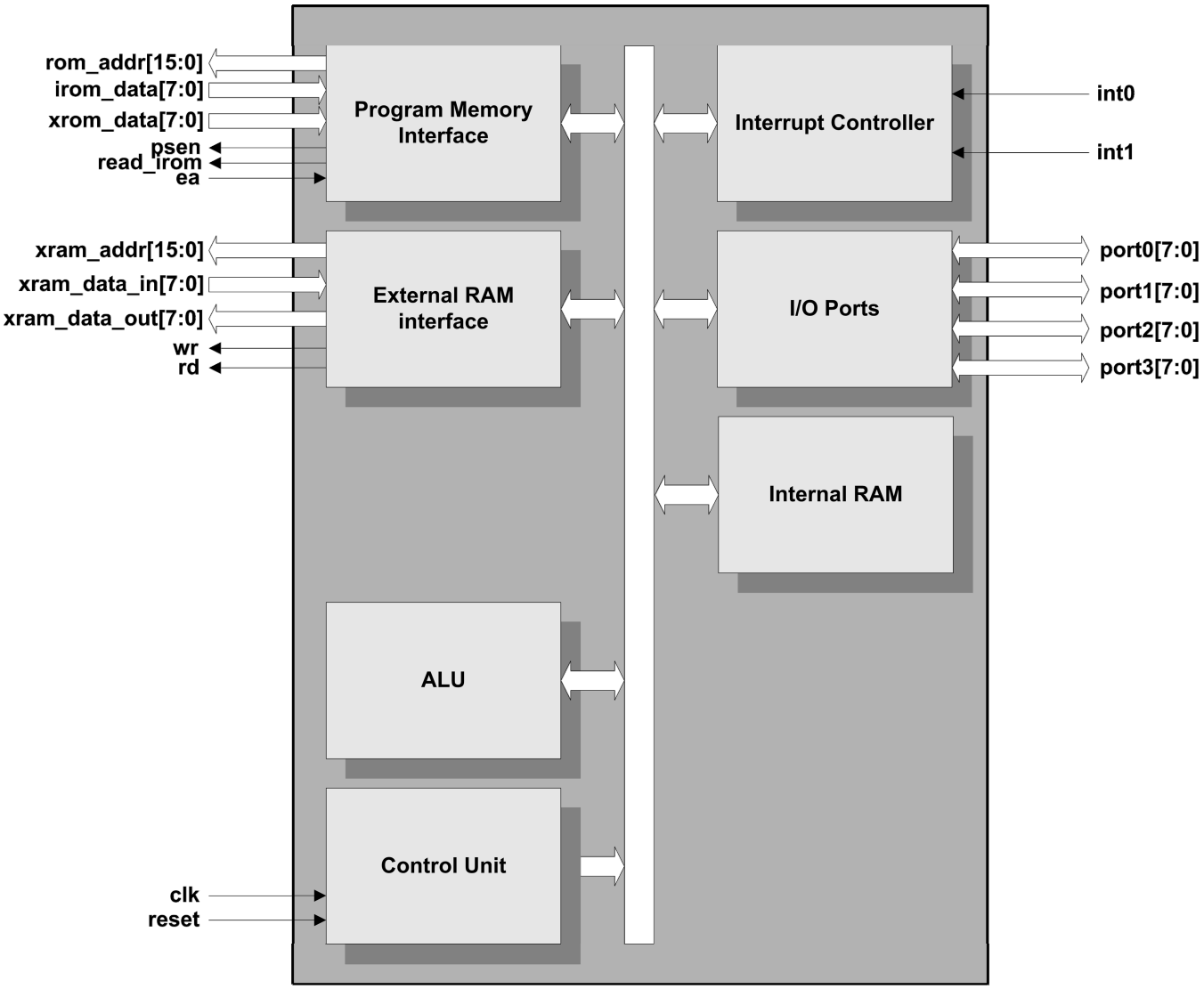


Pin Description

Name	Signal Direction	Description
I/O Ports		
port0_in[7:0]	Input	Port 0 input bus.
port0_out[7:0]	Output	Port 0 output bus.
port1_in[7:0]	Input	Port 1 input bus.
port1_out[7:0]	Output	Port 1 output bus.
port2_in[7:0]	Input	Port 2 input bus.
port2_out[7:0]	Output	Port 2 output bus.
port3_in[7:0]	Input	Port 3 input bus.
port3_out[7:0]	Output	Port 4 output bus.
Interrupts		
int0	Input	External interrupt 0 source. If level activated, active low interrupt 0. If transition activated, active on falling edge.
int1	Input	External interrupt 1 source. If level activated, active low interrupt 1. If transition activated, active on falling edge.
System Signals		
clk	Input	System clock signal.
reset	Input	Global reset signal.

Program Memory Interface		
rom_addr[15:0]	Output	Program memory address bus.
irom_data[7:0]	Input	Internal program memory data bus.
xrom_data[7:0]	Input	External program memory data bus.
psen	Output	Read strobe to external program memory.
irom_read	Output	Read strobe to internal program memory.
ea	Input	External Access enable.
External Data Memory Interface		
xram_addr[15:0]	Output	External RAM address bus..
xram_data_in[7:0]	Input	External RAM data bus input.
xram_data_out[7:0]	Output	External RAM data bus output.
wr	Output	External RAM write enable.
rd	Output	External RAM read enable.

Block Diagram



Functional Description

The previous diagram shows all major so_ip_8051C256 modules described here in more detail.

Program Memory Interface

- Can address up to 64K bytes of internal (on chip) program memory.
- Can address up to 64K bytes of external (off chip) program memory.

Program memory interface contains logic necessary for efficient interfacing to program memories. so_ip_8051C256 has two program memory spaces, small internal, and large external memory. Size of internal program memory is set to 4K bytes, when core is delivered, but this can be modified by user's request to any value up to the 64K bytes. Typically, internal memory is implemented as on-chip memory, and external memory is implemented as off-chip memory. It is important to emphasize that this does not have to be

so. Both memories can be implemented as on-chip or as off-chip memories, depending on user preferences.

External RAM Interface

- Can address up to 64K bytes of external data memory

External RAM interface contains logic needed to implement access to external RAM memory. Typically this memory is implemented as off-chip, but there is no problem if user wants to implement it as on-chip module.

Internal RAM

- Can address up to 256 bytes of internal (on-chip) RAM memory

Contains 256 bytes of internal RAM and control logic that enables easy access. Upper 128 bytes can be accessed using indirect addressing only. Part of this memory is also bit-addressable. This is the same RAM that can be found in original 8051 microcontroller.

ALU

- 8-bit arithmetic and logic operations
- Integrates complete Boolean processor
- 8x8 bit unsigned multiplication
- 8/8 bit unsigned division

ALU unit implements all of the arithmetic and logic functions that can be found in 8051 microcontroller. These are: addition, subtraction, multiplication, division, logical AND, OR and XOR operations. ALU also contains a complete Boolean processor that operates with single bit operands.

Control Unit

Control unit performs instruction fetch, decoding and execution. Also it controls the operation of entire system.

Interrupt Controler

Interrupt controller has two external interrupt sources. There are two priority levels that can be assigned to each of the interrupts. Also each source has an independent priority bit, flag bit, interrupt vector and enable bit. There is global enable bit that enables or disables all of the interrupts.

I/O Ports

so_ip_8051C256 provides user with four 8-bit input/output ports, Port0-Port3. Each port is both bit-addressable or can be addressed as a byte.

Verification Methods

so_ip_8051C256 was tested both in VHDL simulator and in dedicated hardware platform. First, every module of the so_ip_8051C256 core was individually tested to verify correct operation. Next, special test programs were written to test each of the instructions from the instruction set of 8051 microcontroller, correct interrupt handling and correct operation of timers and serial port.

Device Utilization & Performance

Supported Family	Device	Optimized for Speed			Optimized for Area		
		Slices	IOs	F_{max} (MHz)	Slices	IOs	F_{max} (MHz)
Spartan-II	2S200-6	1296	137	50	1136	137	40
Spartan-IIE	2S200E-6	1297	137	50	1141	137	42
Spartan-3A	3S1400A-5	1369	137	70	1193	137	62
Virtex	XCV400-6	1304	137	46	1145	137	40
Virtex-E	V200E-8	1344	137	55	1139	137	46
Virtex-II	2V500-6	1339	137	93	1186	137	80
Virtex-II Pro	XC2VP20-7	1359	137	110	1211	137	100
Virtex-4	XC4VLX25-12	1423	137	135	1233	137	120
Virtex-5	XC5VLX30-3	567	137	185	537	137	155

Notes:

1. All core I/O signals are routed off chip
2. Results were obtained using Xilinx ISE 10.3i version of software

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/10/2009	1.0	Initial release.