7 Series FPGA Transceivers

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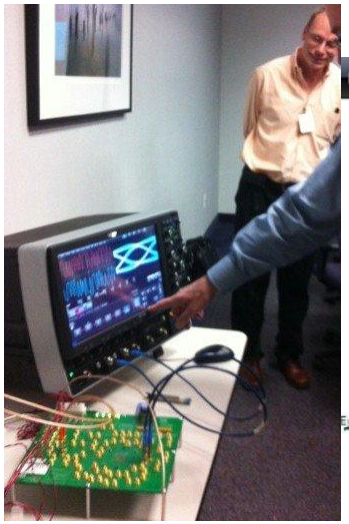
SO-Open-Days, Vienna December 2012

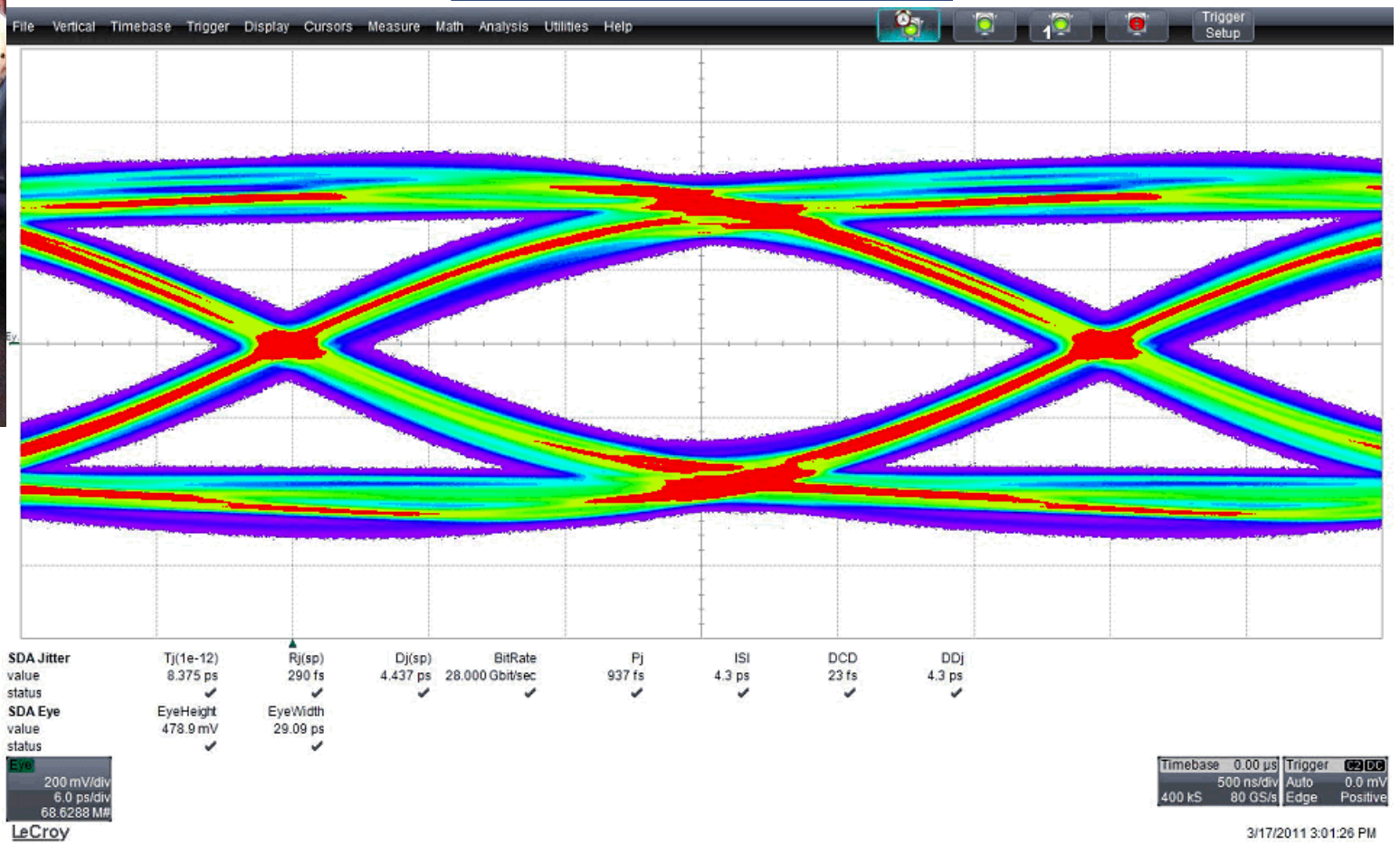
Agenda

- **Why Transceivers?**
  - Update on 7-Series Status – first 28nm FPGAs shipping since March!
- **Transceiver Overview**
- **Transceiver Architecture**
  - Block Diagrams + Supported Protocols
  - Optics Support
  - Backplane Support
  - 28Gbps Support (special section)
- **7 Series Overview**
  - Family Tables
  - Schedule
- **Summary**

GTZ 28G Serdes Test Chip
LC Tank PLL Eye Diagram

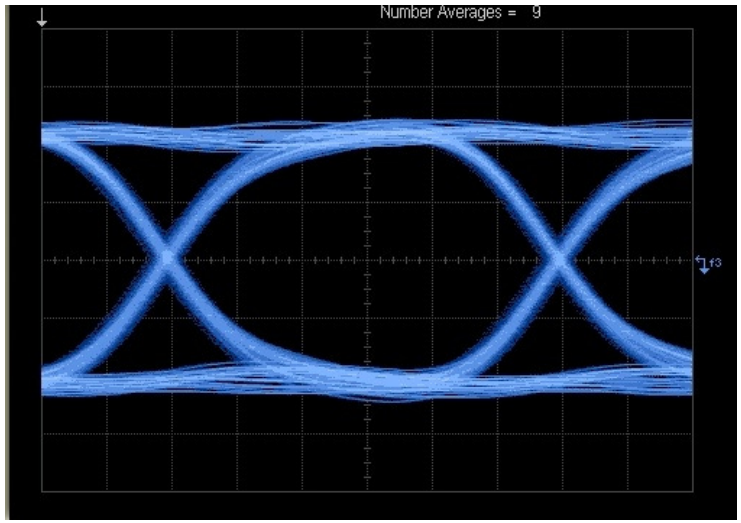


28G SERDES Performance



- Bit Rate 28Gbps
- Rj = 290 fs
- Tj = 8.375 ps
- 200 mv/div
- 6.0 psec/div
- 68 Mbits

  of capture data



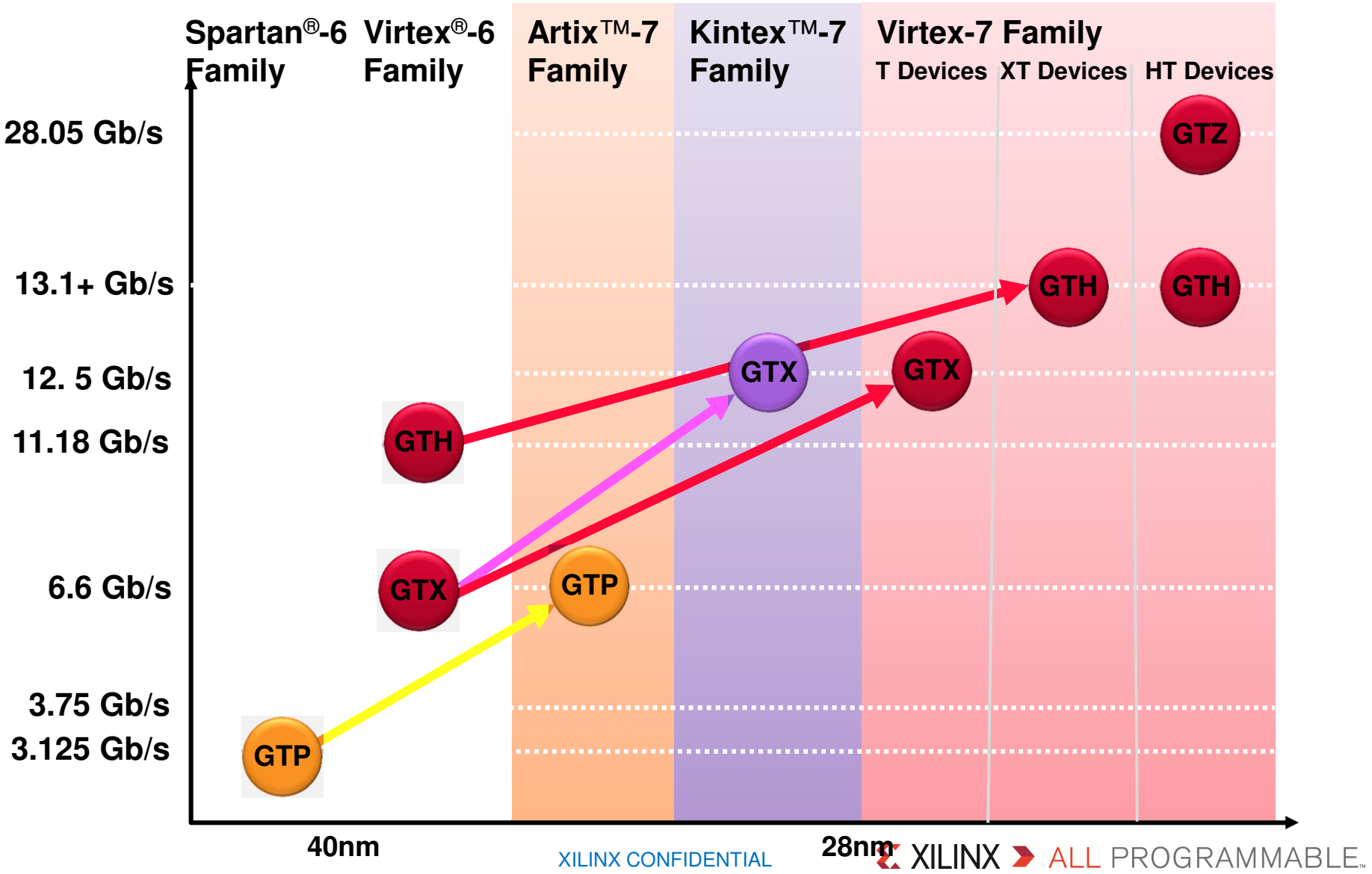
	10G SFP+ Spec	Xilinx 7series GTX	
Random Jitter (Rj) @ 1^-12	0.15UI	0.09 UI	✓
Deterministic Jitter (Dj)	0.15UI	0.06 UI	✓
Total Jitter (Tj)	0.28UI	0.15 UI	✓

Period: 97ps (10.3125Gbps)
TJ: 14.78ps @ 1e-12 BER (15%)
RJ: 654.30fs (9%)
DJ: 5.62ps (6%)

DISCLAIMER!
This data is very early, typical silicon and based on 1 week of testing!

Transceiver Overview

7 Series Transceiver Roadmap
40nm => 28nm Roadmap



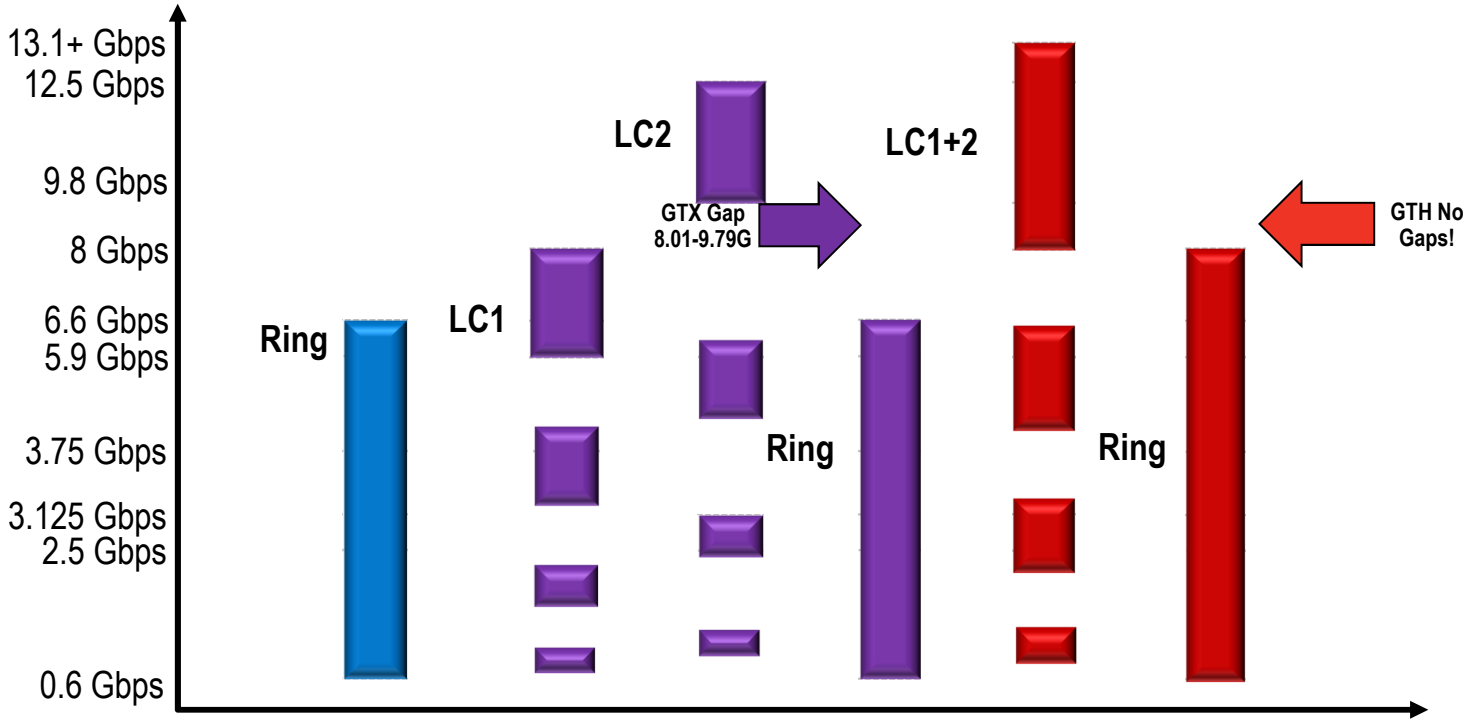
7 Series Min/Max Performance by Package/Speed Grade

Speed Grade	Artix GTP			Kintex GTX			Virtex GTX		Virtex GTH		Virtex GTZ	
	min	max (FB, CS)	max (FF)	min	max (FB, CS)	max (FF)*	min	max	min	max	min*	max
-1 C/I LE	0.5	3.75	3.75	0.5	6.6	6.6	0.5	6.6	0.5	8.5	2.45	25.78
-2 C/I LE	0.5	5.4	6.6	0.5	6.6	10.3125	0.5	10.3125	0.5	10.3125	2.45	25.78
-2 E	N/A	N/A	N/A	N/A	N/A	N/A	0.5	10.3125	0.5	11.3	2.45	25.78
- 2 GE	N/A	N/A	N/A	N/A	N/A	N/A	0.5	12.5	0.5	13.1	2.45	28.05
-3 E	0.5	5.4	6.6	0.5	6.6	12.5	0.5	12.5	0.5	13.1	N/A	N/A

Notes:

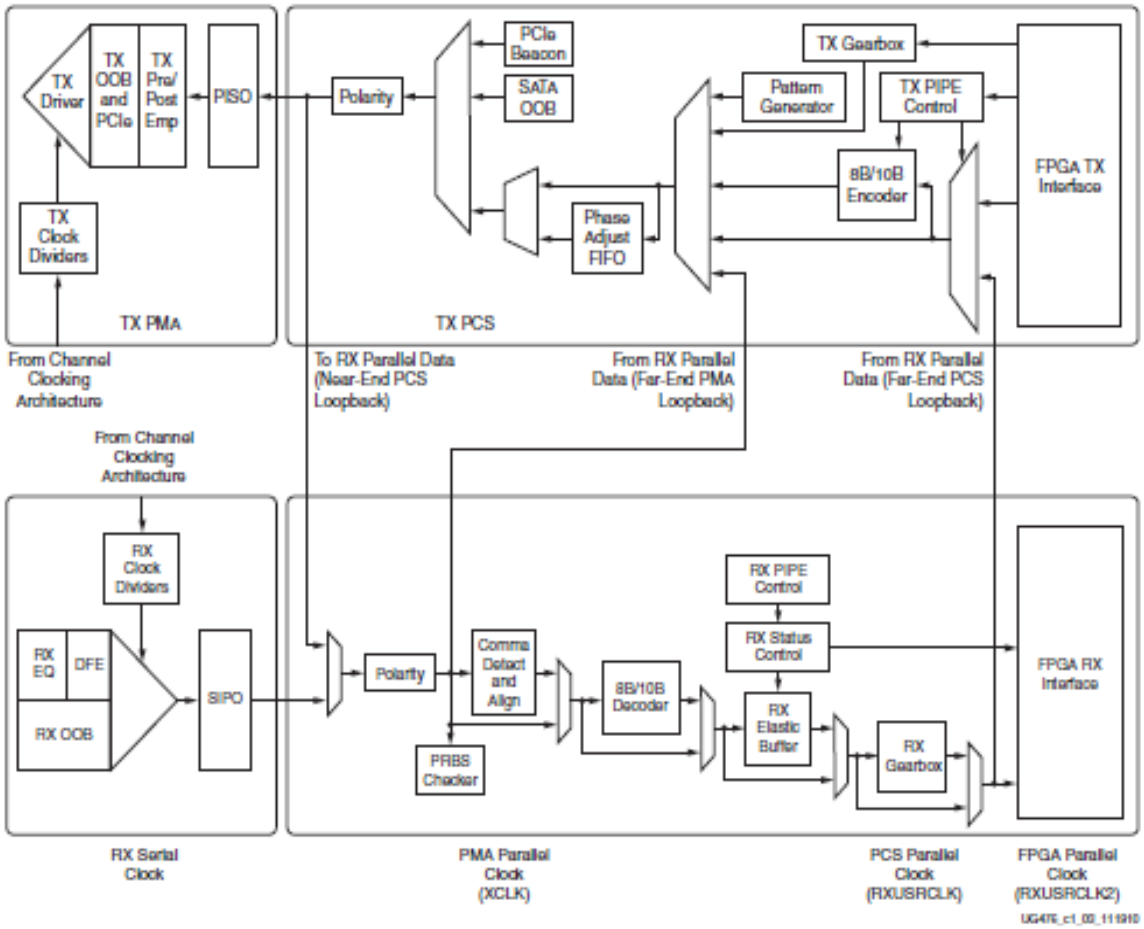
- This table describe max/min rates, more details in the following slides
- 10G+ performance in K7 requires FF package (lidded flipchip)
- E temp grade is 0'C – 100'C temp range
- GTZ frequency range is 19.6G to max with /2, /4 and /8 dividers
- Rates from 500Mbps to 0Mbps can be supported with XAPP875

7 Series Transceiver Architecture
PLL Range (-3E speed grade)



Divider	Artix7 GTP		Kintex7/Virtex7 GTX			Virtex7 GTH	
	LC	Ring	LC1	LC2	Ring	LC1+2	Ring
/1	N/A		5.9-8.0	9.8-12.5		8.0-13.1	
/2	N/A		2.9-4.0	4.9-6.25		4.0-6.55	
/4	N/A		1.45-2.0	2.4-3.125		2.0-3.25	
/8	N/A		0.7-1.26	1.2-1.56		1.0-1.6	
		0.6-6.6			0.6-6.6		0.6-8.0

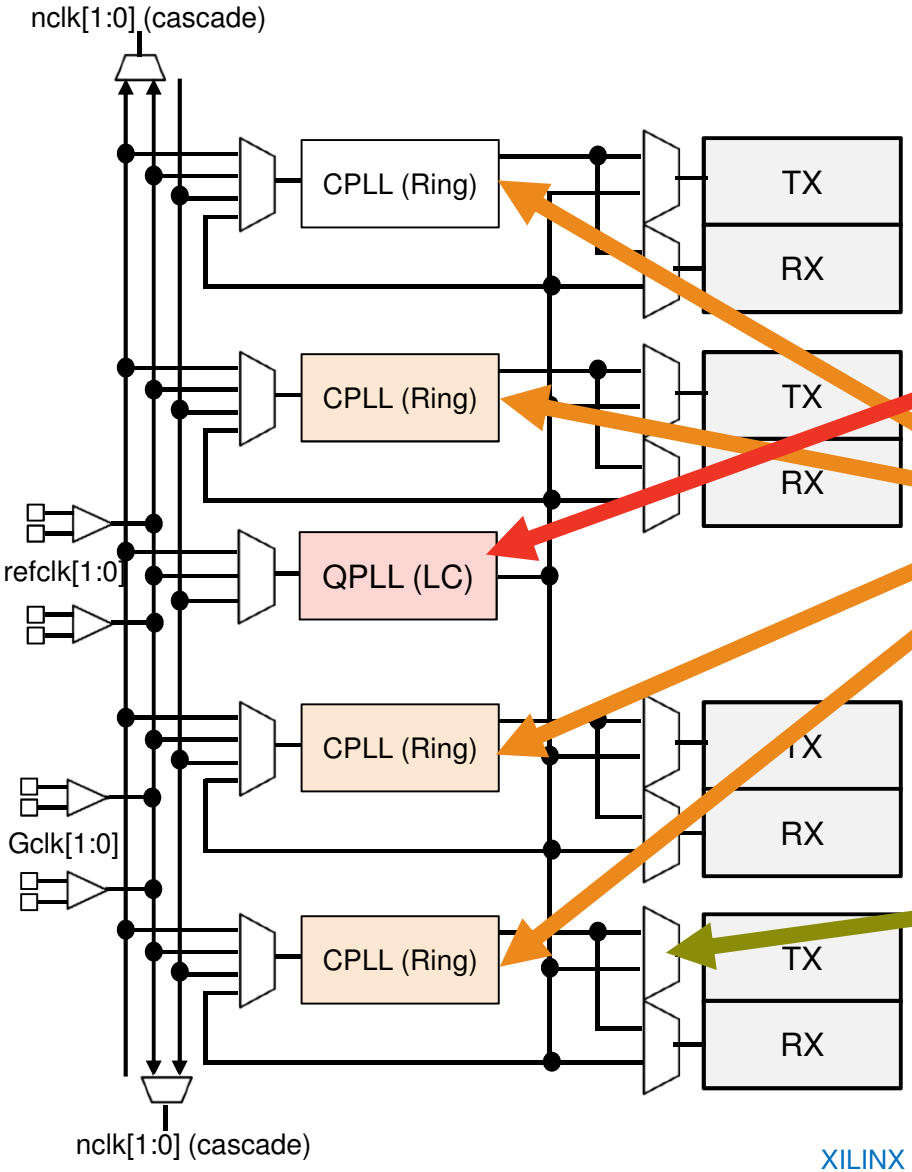
7 Series Architecture
Block Diagram of a Single Channel (GTX)



- **One "channel" is one TX and one RX**
- **Key Features:**
  - Datapaths:
    - 0G to 12.5G* for GTX
  - Equalization:
    - TX Pre/Post Emphasis
    - RX AGC
    - RX CTLE (linear EQ)
    - RX DFE
  - Debug/Test
    - Hard Logic PRBS gen/check
    - 2D eyescan

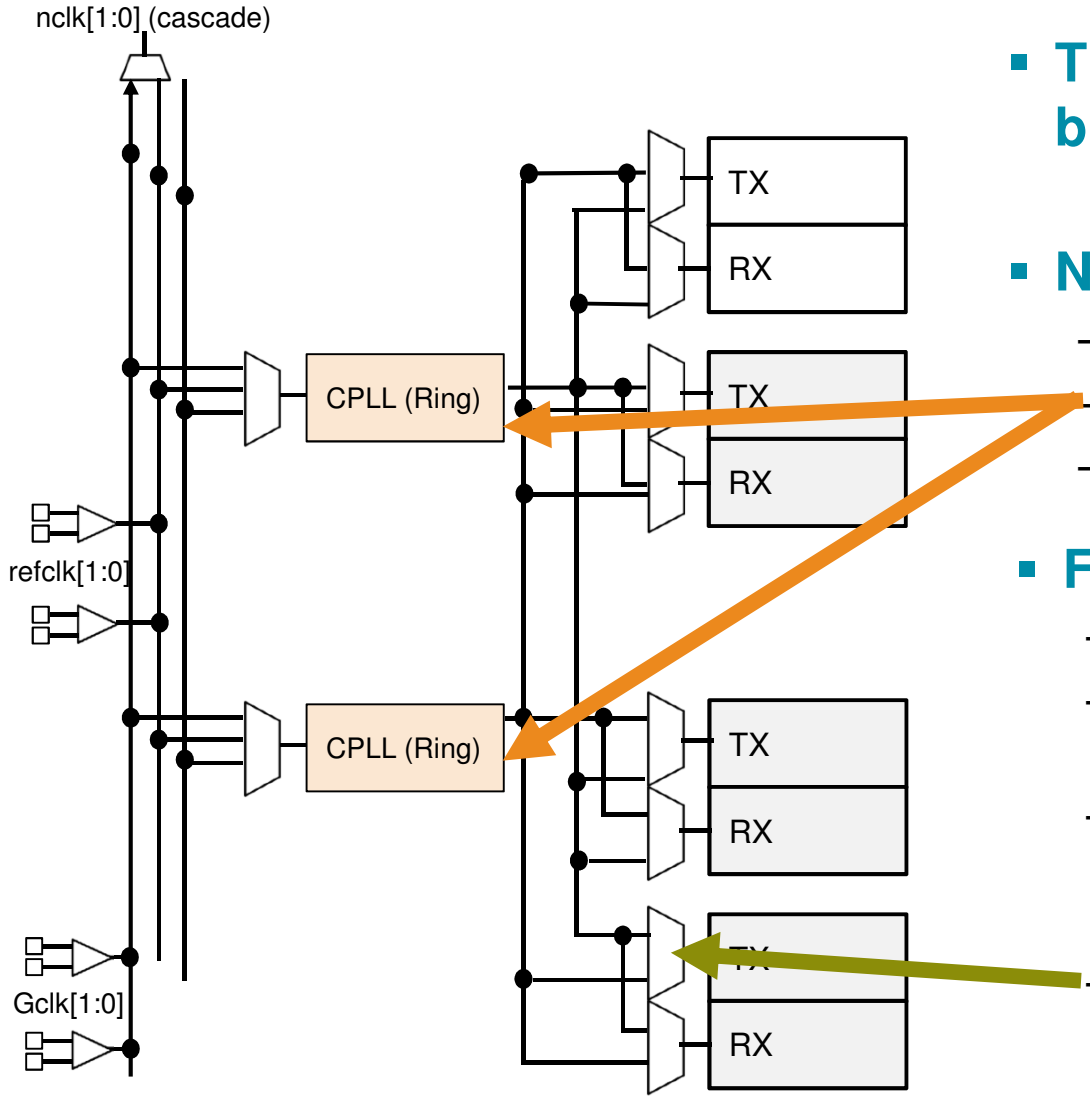
*** 0G – 0.499G requires XAPP 875**

7 Series GTX and GTH Transceiver Architecture
Block Diagram of Transceiver Quad



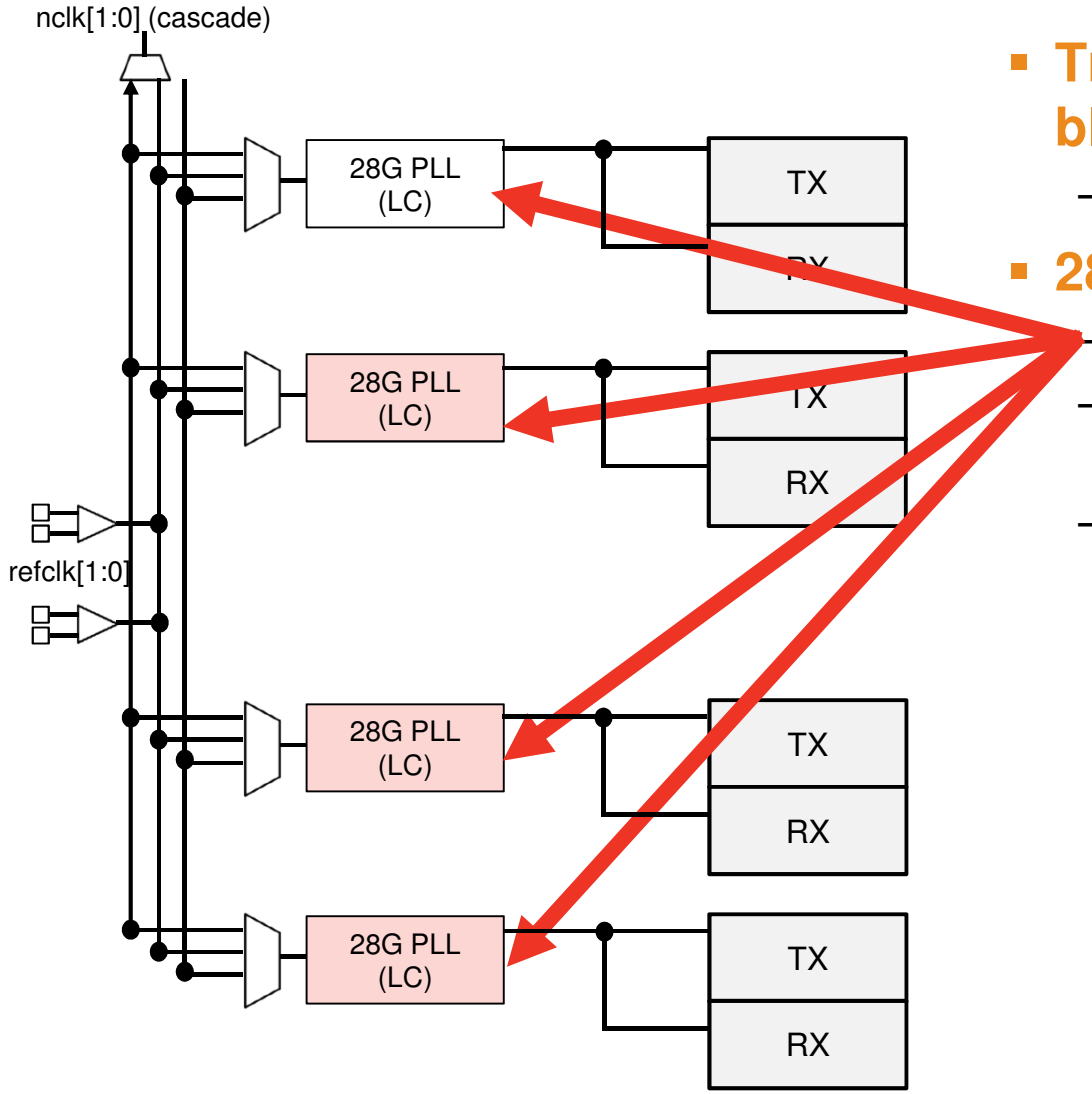
- **Transceivers in Quads (4 per block)**
  - 1 or 2 columns of Transceivers
- **New PLL Architecture**
  - LC Tank shared (high performance)
    - LC can operate at 1/2, 1/4 and 1/8 rate
    - 2 LC = wider freq. (mutually exclusive)
  - Ring Oscillator x4 (wide range)
- **Flexibility**
  - Allows async operation between TX and RX by use of the Ring for TX and the LC tank for RX (or vice versa)
  - Unused PLLs can be powered down
  - One mux per direction with independent select lines

7 Series GTP Transceiver Architecture
Block Diagram of Transceiver Quad



- **Transceivers in Quads (4 per block)**
- **New PLL Architecture**
  - No LC Tank (lower area)
  - Ring Oscillator x2 (wide range)
  - GCLK reference possible for low rate protocols
- **Flexibility**
  - 2 protocol / quad
  - Allows everything to run off of 1 PLL for low power
  - This allows async operation between TX and RX by use of one Ring for TX and one ring for RX (or vice versa)
  - One mux per direction with independent select lines
  - Separate divider per TX/RX

7 Series GTZ Transceiver Architecture
Block Diagram of Transceiver Octal



- **Transceivers in Quads (4 per block)**
  - 1 LC tank PLL/channel
- **28G-focused PLL Architecture**
  - 1 LC tank PLL/channel
  - No high speed muxing
    - lowest jitter
  - SFI-S skew alignment across up to 8 channels

7 Series Transceiver Architecture
Major Supported Protocols

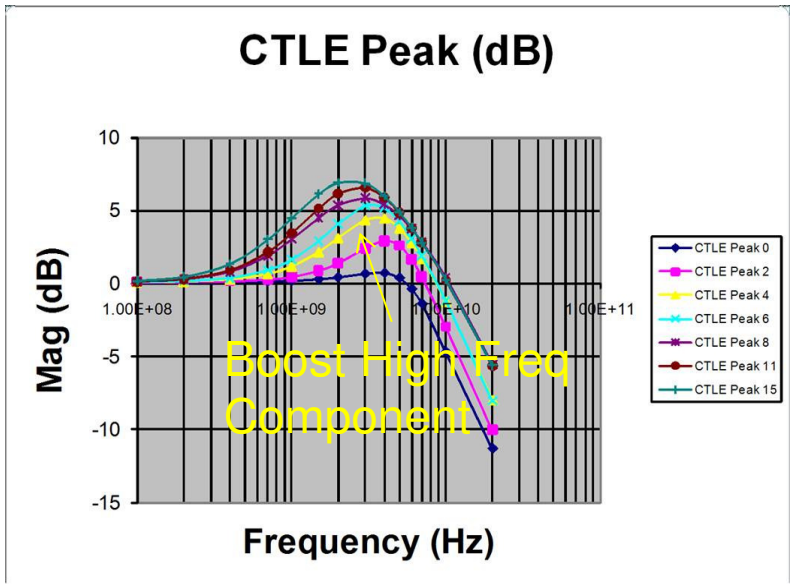
Market	Protocol	Artix-7 GTP	Kintex-7/Virtex-7 GTX	Virtex-7 GTH	Virtex-7 GTZ
General	PCI Express	Gen1, 2	Gen1, 2, 3	Gen1, 2, 3	(supported on GTH)
Wired	Ethernet	1GE, 2.5GE, XAUI, RXAUI	1GE, 2.5GE, XAUI, RXAUI, 10GBase-R, 10G-KR*, 40GE, 100GE	1GE, 2.5GE, XAUI, RXAUI, 10GBase-R, 10G-KR (enhanced), 40GE, 100GE	100GE (25.7G)
	SONET/OTU	OC-3/12/48	OC-3/12/48/192, OTU1/2/3/4	OC-3/12/48/192, OTU1/2/3/4	OTU4 w 7% FEC (27.95G) SFI-S, OTL4.4
	Interlaken	<= 6.6G	<=6.5G, 10.3125G 12.5G	<=6.5G, 10.3125G, 12.5G	20.625G (2x10.3125), 25G (2x12.5G)
	Custom Backplane	<= 3.125G	<=6.5G, CEI-11-LR*	<= 6.5G, CEI-11LR (enhanced)	(supported on GTH)
	PON	BPON, GPON, GEPON (up to 1.25 BCDR)	BPON, GPON, GEPON, 10GEPON, 10GGPON (up to 2.5G BCDR)	BPON, GPON, GEPON, 10GEPON, 10GGPON	(supported on GTH)
Wireless	CPRI/OBSAI	0.614, 1.2, 2.4, 3.0, 4.9, 6.6	0.614, 1.2, 2.4, 3.0, 4.9, 6.14, 9.8, 12	0.614, 1.2, 2.4, 3.0, 4.9, 6.14, 9.8, 12	2.4, 3.0, 4.9, 6.0, 9.8, 19.6, 24
	Serial Rapid IO	Gen1, 2	Gen1, 2	Gen1, 2	(supported on GTH)
Audio Video[2]	SDI	SD/HD/3G-SDI	SD/HD/3G-SDI/10G-SDI	SD/HD/3G/10G-SDI	(supported on GTH)
	DisplayPort	1.6, 2.7, 5.4	1.6, 2.7, 5.4	1.6, 2.7, 5.4	(supported on GTH)
Other	QPI	x	4.8, 6.4`	4.8, 6.4, 8.0, 9.6	(supported on GTH)
	Fiber Channel	1G, 2G	1G, 2G, 4G, 10G	1G, 2G, 4G, 8G, 10G	FC32 (28.05G), FC20, FC16, FC10
	SATA/SAS	1.5G, 3G, 6G	1.5G, 3G, 6G	1.5G, 3G, 6G	(supported on GTH)
	Aurora	Up to 6.6G	Up to 12.5G	Up to 13.1G	Up to 28.05G

Optical Interfaces Optics Support: what is planned.

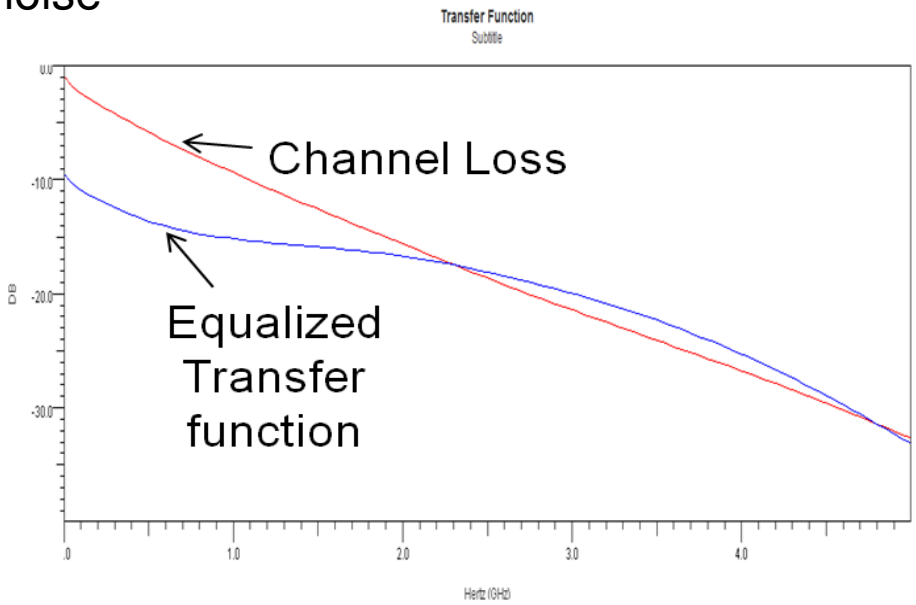
			40nm	28nm			
Protocol	**Module**	**Notes**	**V6 HXT GTH**	**A7 GTP**	**K7/V7 GTX**	**V7 GTH**	**V7 GTZ**
100GE/OTU4	CFP	10x10.3G / 10x12.5G	✓		✓	✓	
	CXP	10x10.3G / 10x12.5G	✓		✓	✓	
	CFP2	4x25.78G / 4x27.95G					✓
40GE/OTU3	300pin	17x2.488G			✓	✓	
	(lim)QSFP	4x10.3125G	✓		✓	✓	
10GE/OTU2/OC 192/FC10/ CPRI9.8/6/4.9/3	(lim)SFP+	1x9.95G / 1x10.3G / 1x10.5G / 1x10.7G / 1x11.3G / 1x9.8/6/4.9/3	✓		✓	✓	
	XFP	1x9.95G / 1x10.3G / 1x10.5G / 1x10.7G / 1x11.3G / 1x9.8G	✓		✓	✓	
	XENPAK	4x3.125G	✓	✓	✓	✓	
GigE / OC-48/12/3 FC 4/2/1	SFP	1x1.25G / 1x2.488G / 1x0.622G / 1x0.155G	✓	✓	✓	✓	

Backplanes and Equalization
Technique #1: Linear Equalization

- **Linear Equalization**
  - Transmitter: Attenuate low frequency and/or boost high frequency
  - Receiver: Boost high frequency
  - Compensate insertion loss
  - Limitation: Boost high frequency noise



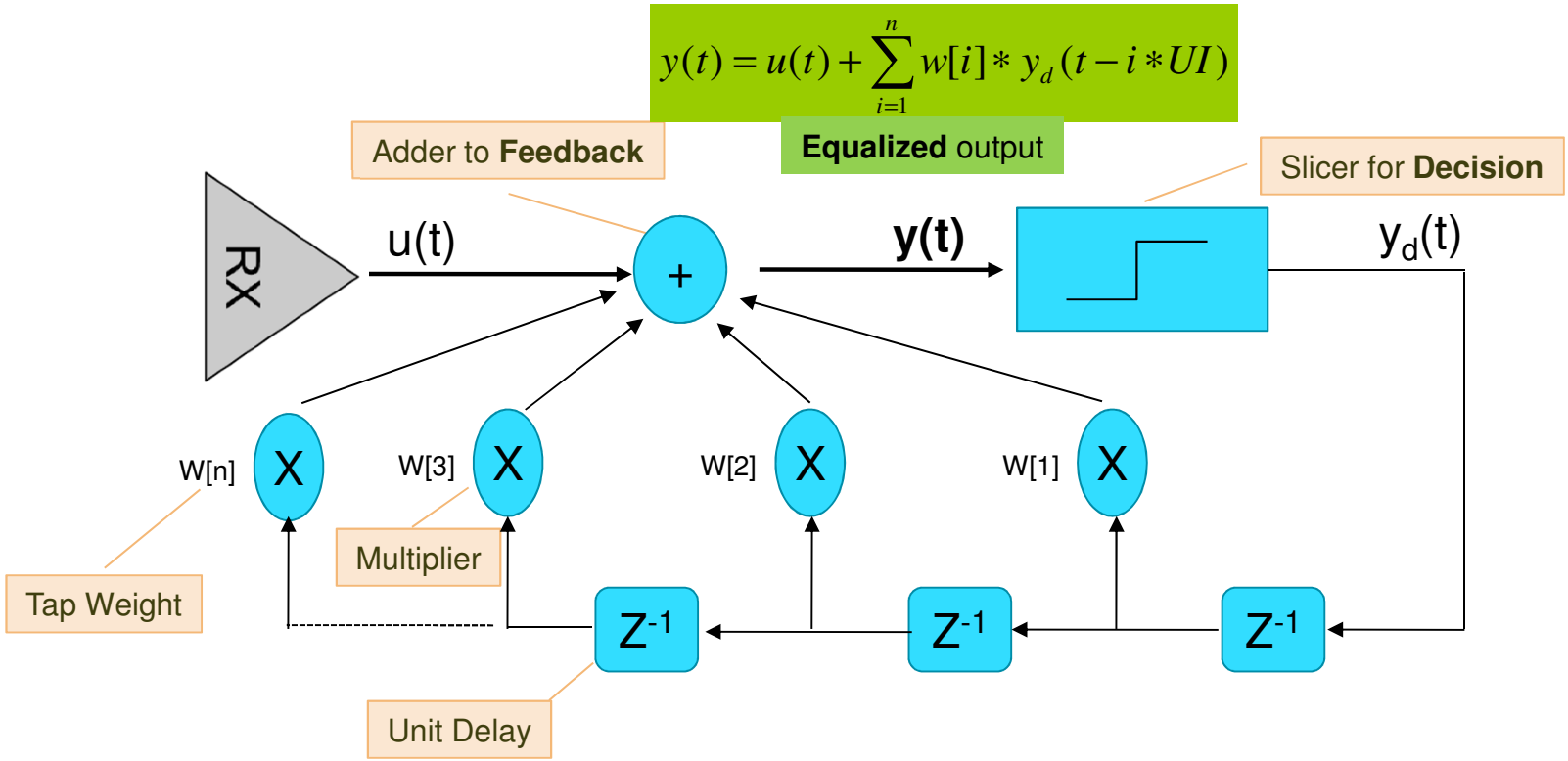
RX linear equalizer frequency response



TX pre-emphasis attenuate low frequency & boost high frequency

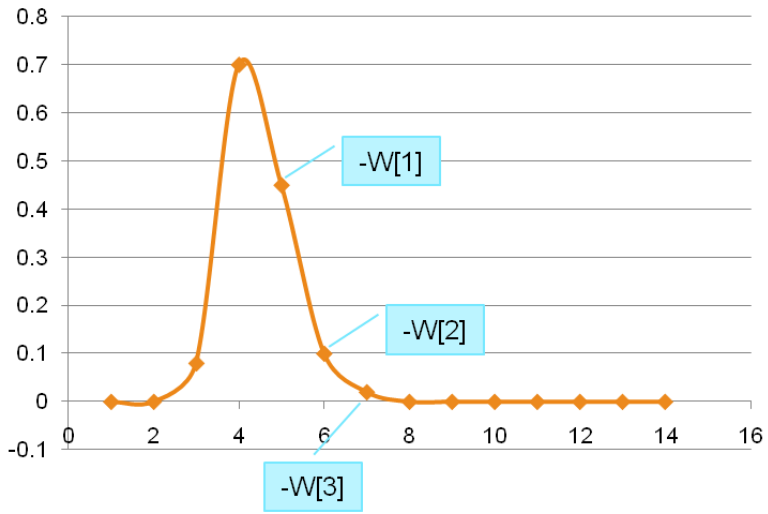
Backplane and Equalization
Technique #2: Decision Feedback Equalization

- **Decision Feedback Equalization (DFE)**
  - A nonlinear equalizer that uses previous symbols to eliminate the Inter-Symbol-Interference (ISI) on current symbol.
    - The ISI on current symbol, caused by previous symbols, is subtracted by DFE.



Backplane and Equalization
DFE Challenge and Limitation

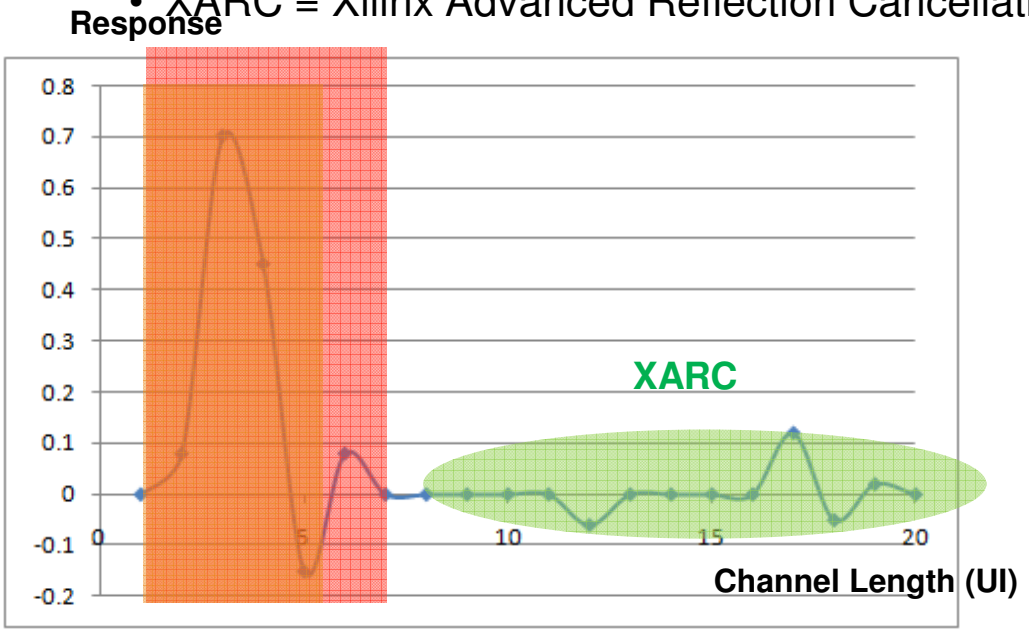
- **Tap weight**
  - Ideal tap weights
  - LMS Adaptation
- **Error propagation**
- **Speed requirement**



Tap weight based on ISI

Backplane and Equalization
XARC – Xilinx Advanced Reflection Cancellation

- **DFE for Reflection**
  - Regular DFE cancels reflections near the package
  - Virtex-7 GTH with DFE + XARC cancels reflections farther in the channel
    - XARC = Xilinx Advanced Reflection Cancellation



Xilinx Kintex/Virtex GTX

Xilinx Virtex-7 GTH 7 fixed + XARC

Backplanes and Equalization
Backplane Support with 7-Series

Geometry	40nm	28nm	
Parameter	**V6 HXT**	**K7/V7GTX**	**V7GTH**
Max Rate	11.18 (LC)	12.5	13.1
LC Tank	11.18	12.5	13.1
TX Jitter (all 10 lanes)	< 0.28 UI	0.15 UI typ (preliminary)	TBD (equal or better to GTX)
TX Pre/Post emphasis	Yes	Yes	Yes
RX Linear EQ	Adaptive	Adaptive	Adaptive
RX DFE #taps	3	5	11 (7 fixed + 4 sliding up to 50)
RX DFE Adaptive Y/N	Adaptive (3rd gen)	Adaptive (4th gen)	Adaptive (5th gen)
10G-KR support Y/N	No (IP tested @ UNH)	Good	Best
Internal Eyescan Y/N	1D (3rd gen)	2D (4th gen)	2D (5th gen)

Significant Improvements in 10G Long-Reach Support for 28nm!

V7 GTH will be the best backplane transceiver in any FPGA

7-series Transceiver Tools

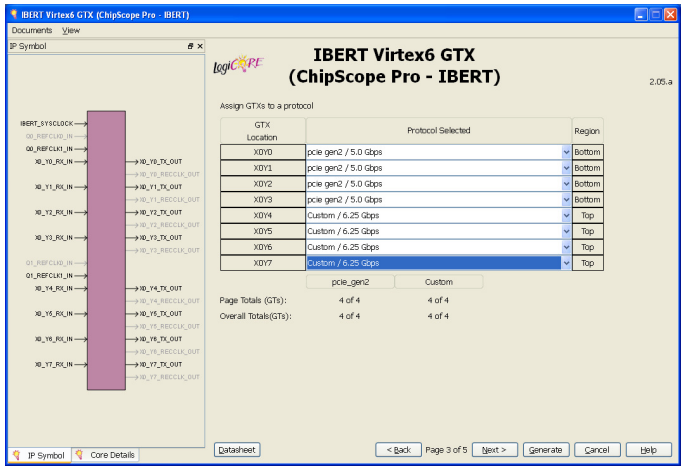
Transceiver Tools
A Note on Tools and Usability

- **Xilinx-generated IP cores**
  - Xilinx engineers encapsulate the Transceiver in their cores
  - Easier for customers and prevents misconfiguration
  - Examples: PCIe, 10GE, Interlaken, CPRI, SDI, etc.

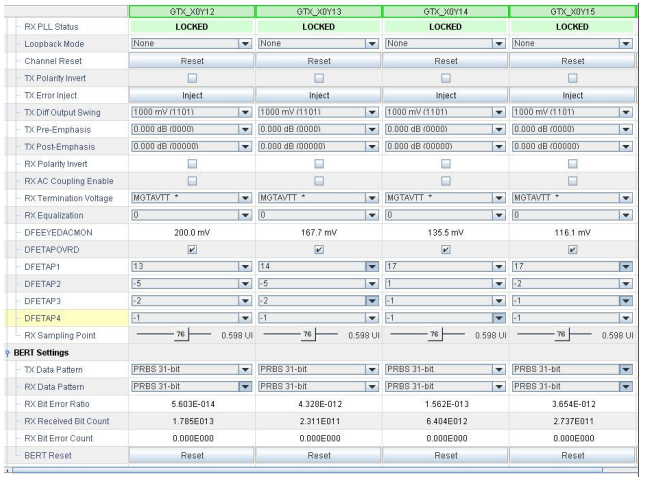
- **Xilinx Transceiver Wizard**
  - Allows pre-configured settings for common protocols
  - Allows GUI-based customization for customer protocols
  - Performs clocking and other transceiver connectivity DRCs

- **Xilinx Chipscope IBERT**
  - Allows hardware evaluation of backplanes with the real FPGA
  - Allows in-system debug for system bringup and manufacturing burn-in
  - IBERT GUI Key Features
    - Hardware PRBS Generator/Checker
    - Eye Height and TX Pre-emphasis adjustment
  - Eyescan allows margining of channel in Hardware

Transceiver Tools
IBERT - Integrated Bit Error Rate Tester

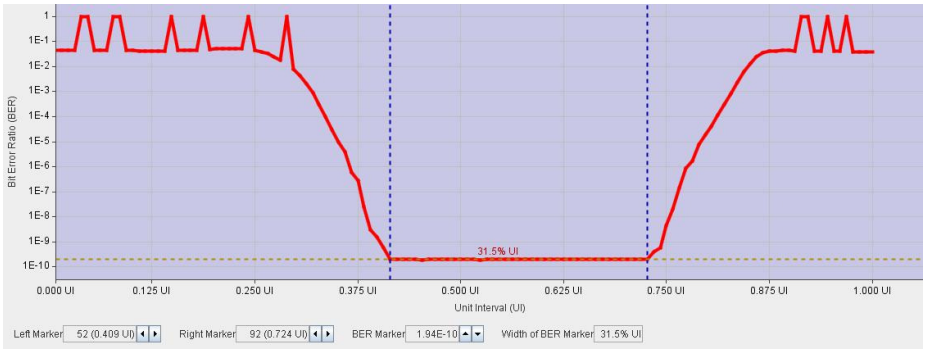


IBERT Generator GUI
Targets the FPGA on your board



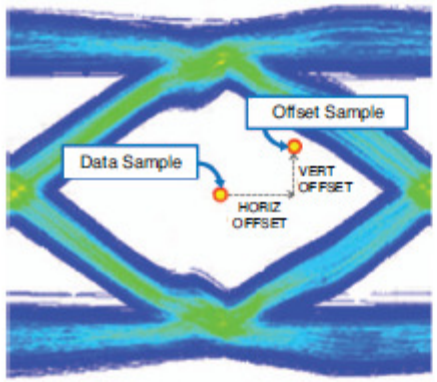
Run time GUI
Controls the transceivers on your board
Adjust all transceiver parameters - swing

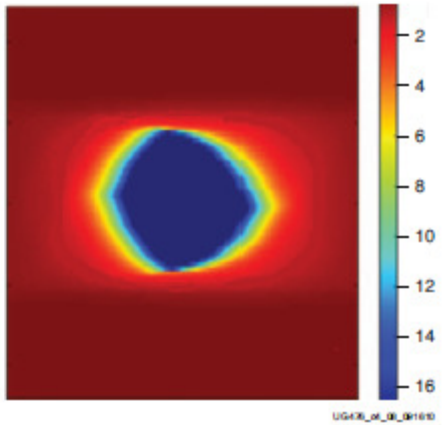
- 6 Series Bathtub plots from run time GUI
- 7 Series will be statistical eye using non-destructive eye monitor
- Gives you relative measurements of channel margin and EQ performance

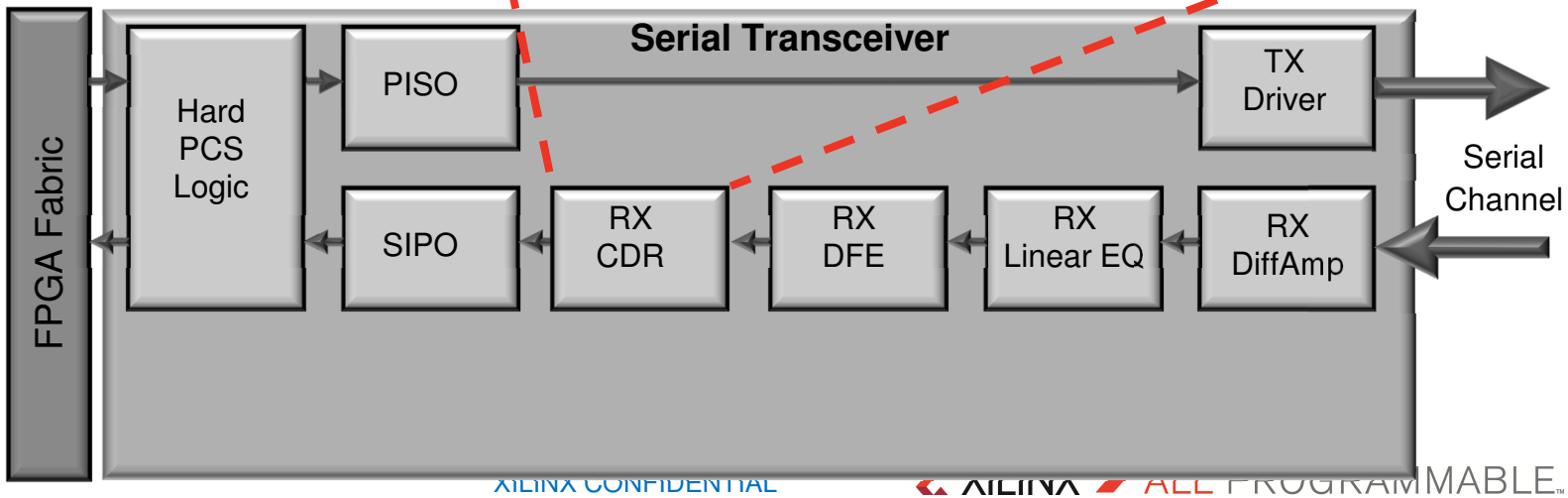


Transceiver Tools:
7-Series Chipscope w. IBERT and Eye Scan)

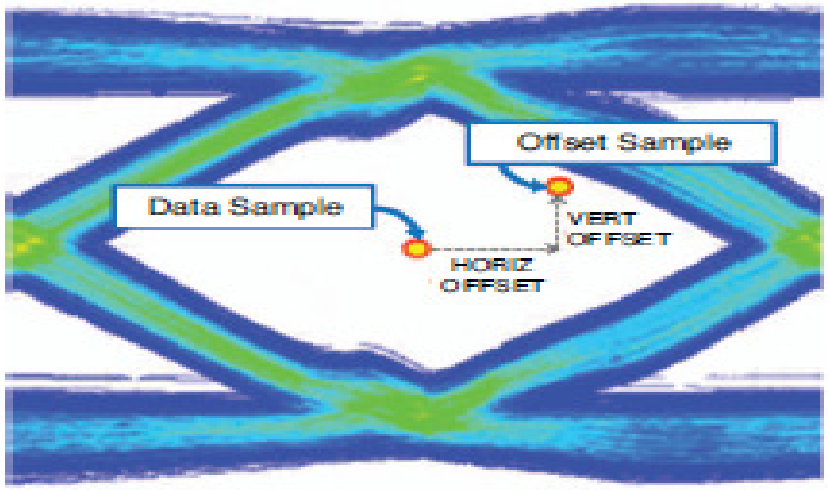
- **Look inside the receiver!**
  - View Post-EQ eye
  - Measure and extrapolate BER!
  - Non-destructive scanning on live data!
- **Proven Xilinx Technology**
  - 5th generation eye scan
  - 2D eye plot (T and V)

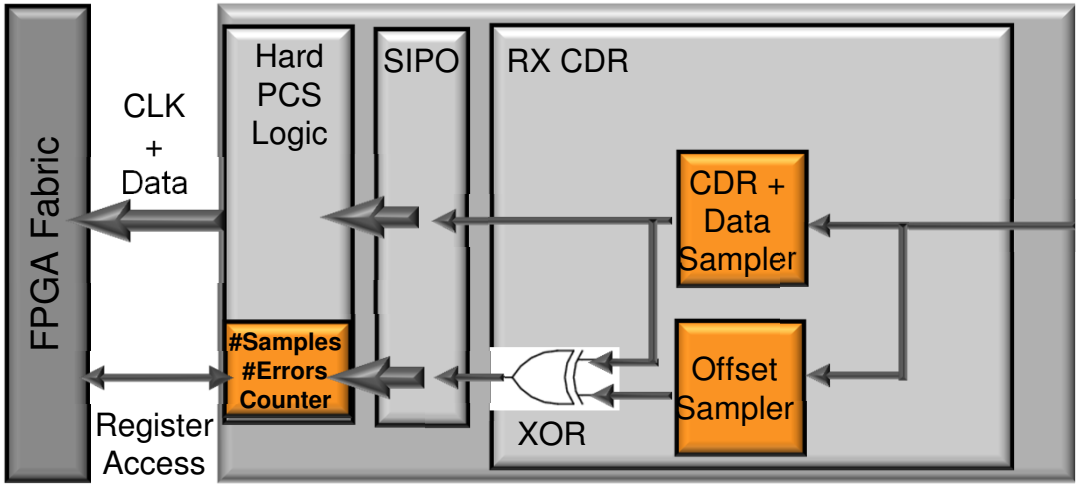






Transceiver Tools: How Does Non-Destructive Eye Scan Work?

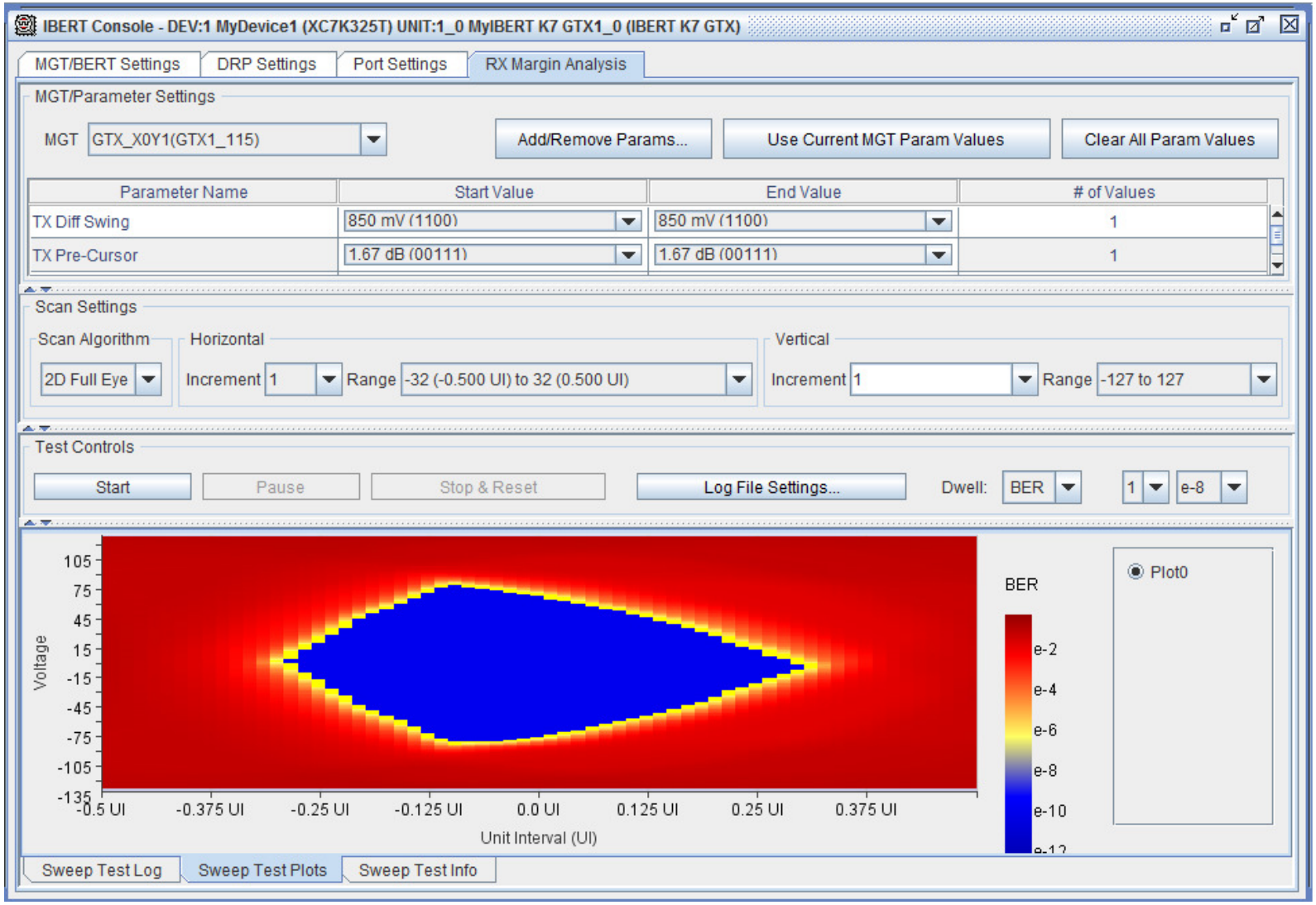




- **Two Samplers in RX Path**
  - Data Sampler :
    - same as regular CDR
    - Always in center of eye
  - Offset Sampler
    - Moveable sampler to trace the eye
- **If Data and Offset Sampler have different value, a Bit Error has occurred at the Offset Sampler!**
- **# samples and #errors recorded in PCS counter**
- **Allows non-destructive EyeScan on LIVE data w/o creating Data Errors**

Data	Offset	Bit Error?
0	0	0
0	1	1
1	0	1
1	1	0

Scan Eye 12.5G 156.25MHz refclk (PRBS 7)



Transceiver Tools: How Does Non-Destructive Eye Scan Work?

Application Note: 7 Series FPGAs

XILINX®

XAPP743 (v1.0) October 18, 2012

Eye Scan with MicroBlaze Processor MCS

Author: Mike Jenkins and David Mahashin

Summary

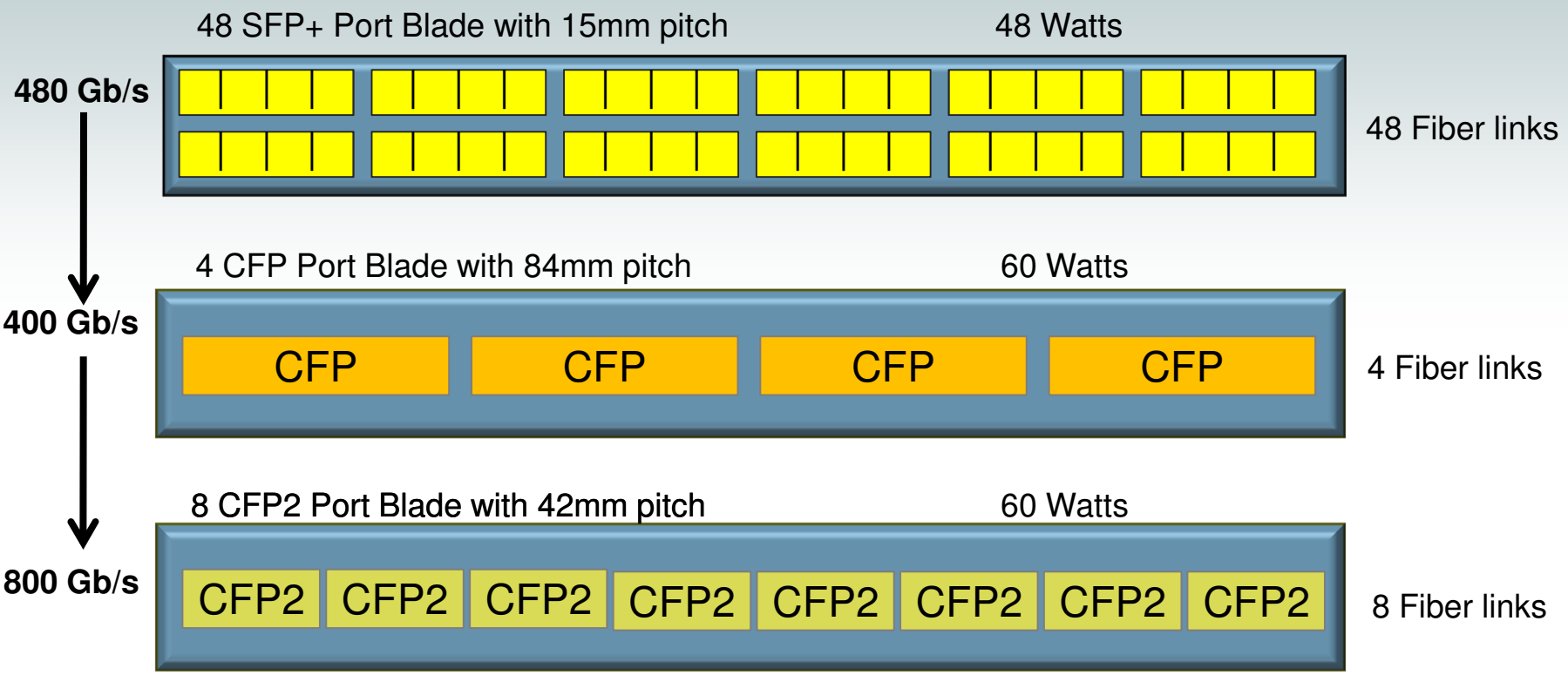
This application note describes code that executes on an internal MicroBlaze™ processor, implementing the algorithm to measure a statistical eye (bit error ratio (BER) versus time and voltage offset) at the post-equalization data sampling point within the receiver of a 7 series FPGA transceiver. Point-by-point measured data is stored in block RAM to be burst read by an external host PC.

Introduction to Eye Scan

As line rates and channel attenuation increase, receiver equalizers are more often enabled to overcome channel attenuation. This poses a challenge to system bring-up because the quality of the line cannot be determined by measuring the far-end eye opening at the receiver pins. At high line rates, the received eye measured on the printed circuit board can appear to be completely closed even though the internal eye after the receiver equalizer is open.

Virtex-7HT
Details on our 28Gbps GTZ Transceiver

Tackling the Power / Bandwidth Density Problem



Power Density is the Primary Limiting Factor To Maximizing Density and Minimize Power Consumption

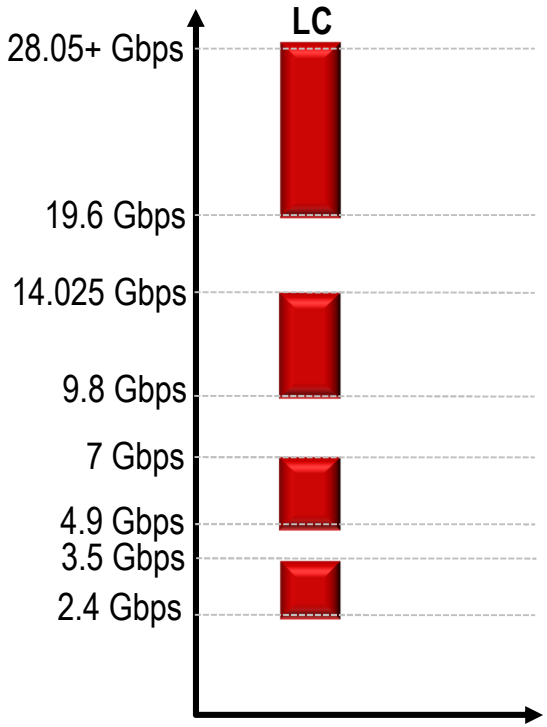
28G GTZ Transceiver
Key Features Summary

- **Wide Range : 28.05G – 19.6G**
  - Full range available in Extended Commercial Temperature Grade (0-100'C)
  - Allows support of "next generation" CPRI @ 19.6Gbps
  - /2, /4 and /8 dividers allow support of 10G and lower datarates
- **Highest Performance : 28G LC Tank Architecture**
  - GTZ purpose-built for highest performance @ 28Gbps for CEI-28G specs
  - One LC/channel for maximum performance (no muxing or fanout)
  - Shared reference clock in quad granularity
- **Designed for Signal Integrity**
  - Proprietary Noise-Isolating Architecture offers nearly 15dB better isolation
  - Ceramic packaging for lowest loss
  - Extra package ground shielding – isolated from SelectIO and GTH transceivers
  - Pinout for interface to 4x28G CFP2 optics (e.g. TX0, TX1, TX2, TX3, RX0, RX1, RX2, RX3)
- **Signal Conditioning Circuitry**
  - Controllable Signal Swing and Pre-Emphasis
  - Auto-Adaptive Equalization to resolve high loss of PCB @ 28G
- **The Industry's Best Serial Debug Tools**
  - Horizontal and Vertical Eyescan tools for channel optimization

GTZ Transceiver
Speed Grade, Frequency Range, Protocol Support

Speed Grade	Virtex-7HT GTZ	
	min	max
-1L C/E	n/a	n/a
-1 C/E	2.4	25.78
-2 C/E	2.4	28.05
-3 E	N/A	N/A

Market	Protocol	Virtex-7HT GTZ
General	PCI Express	(supported on GTH)
Wired	Ethernet	100GE (25.7G)
	SONET/OTU	OTU4 w 7% FEC (27.95G) SFI-S and OTL4.4
	Interlaken	20.625G (2x10.3125) and 25G (2x12.5G)
	Backplane	(supported on GTH)
Wireless	CPRI/OBSAI	2.4, 3.0, 4.9, 6.14, 9.8, 12, 19.6, 24
Other	Fiber Channel	FC32 (28.05G), FC20, FC16, FC10
	Aurora	Up to 28.05G



Divider	Virtex-7HT GTZ
	LC
/1	19.6-28.05
/2	9.8-14.025
/4	4.9 - 7.0
/8	2.4 – 3.5

Artix-7 FPGA Family Table

Artix-7 FPGAs
Optimized for Lowest Cost and Lowest Power Applications
(1.0V, 0.9V)

		Artix-7 SL FPGAs (Advance)				Artix-7 SLT FPGAs (Advance)				Artix-7 T FPGAs	
	Part Number	XC7A200SL	XC7A350SL	XC7A50SL	XC7A75SL	XC7A200SLT	XC7A350SLT	XC7A50SLT	XC7A75SLT	XC7A100T	XC7A200T
Logic Resources	Slices	2,500	5,142	8,300	11,194	2,500	5,142	8,300	11,194	15,850	33,650
	Logic Cells	16,000	32,909	52,480	71,642	16,000	32,909	52,480	71,642	101,440	215,360
	CLB Flip-Flops	20,000	41,136	65,600	89,552	20,000	41,136	65,600	89,552	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kbits)	208	453	688	974	208	453	688	974	1,188	2,888
	Block RAM/FIFO w/ ECC (36Kbits each)	30	65	95	125	30	65	95	125	135	365
	Total Block RAM (Kbits)	1,080	2,340	3,420	4,500	1,080	2,340	3,420	4,500	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	3	4	4	3	3	4	4	6	10
I/O Resources	Maximum Single-Ended I/O	216	216	300	300	216	216	300	300	300	500
	Maximum Differential I/O Pairs	54	54	72	72	54	54	72	72	144	240
Embedded Hard IP Resources	DSP48E1 Slices	60	120	180	240	60	120	180	240	240	740
	PCI Express® [1]	—	—	—	—	1	1	1	1	1	1
	Agile Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)	—	—	—	—	4	4	8	8	8	16
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Package [2], [3] / Dimensions (mm)	Available User I/O: 3.3V SelectIO™ HR I/O, 3.3V SelectIO™ HD I/O Pins (GTP Transceivers)								Available User I/O: 3.3V SelectIO™ HR I/O Pins (GTP Transceivers)	
	CPG236 / 10 x 10	48, 52	48, 52								
	CSG325 / 15 x 15	108, 108	108, 108								
	CSG484 / 19 x 19			144, 156	144, 156						
	CPG237 / 10 x 10					48, 52 (1)	48, 52 (1)				
	CSG324 / 15 x 15									210 (0)	
	CSG325 / 15 x 15					108, 77 (4)	108, 77 (4)	108, 77 (4)	108, 77 (4)		
	CSG484 / 19 x 19					108, 108 (4)	108, 108 (4)	126, 108 (6)	126, 108 (6)		
	FGG484 / 23 x 23									285 (4)	
	FGG485 / 19 x 19							144, 156 (8)	144, 156 (8)		
	FGG676 / 27 x 27									300 (8)	
	FTG256 / 17 x 17									170 (0)	
	SBG484 / 19 x 19										285 (4)
Footprint Compatible	FBG484 / 23 x 23										285 (4)
Footprint Compatible	FBG676 / 27 x 27										[illegible]
	FFG1156 / 35 x 35										00 (16)

XMP086 (v4.2)

CPG: 0.5mm Wire-bond chip-scale; CSG: 0.8mm Wire-bond chip-scale; FTG: 1.0mm Wire-bond fine-pitch; SBG: 0.8mm Lidless flip-chip; FGG: 1.0mm Wire-bond fine-pitch; FBG 1.0mm Lidless flip-chip; FFG: 1.0mm Flip-chip fine-pitch

Notes: 1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Leaded package option available for all packages.
3. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.

Up to 16 Transceivers @ 6.6G

Kintex-7 FPGA Family Table

		Kintex-7 FPGAs Optimized for Best Price-Performance (1.0V, 0.9V)						
	Part Number	XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
Logic Resources	Slices[1]	10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells	65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops	82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kbits)	838	1,938	4,000	4,938	5,663	5,763	6,588
	Block RAM/FIFO w/ ECC (36Kbits each)	135	325	445	715	795	835	955
	Total Block RAM (Kbits)	4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	8	10	6	10	7	8
I/O Resources	Maximum Single-Ended I/O[3]	300	400	500	300	500	350	400
	Maximum Differential I/O Pairs[3]	144	192	240	144	240	168	192
Embedded Hard IP Resources	DSP48E1 Slices	240	600	840	1,440	1,540	1,680	1,920
	PCI Express Interface Blocks[3]	1	1	1	1	1	1	1
	Agile Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTX 12.5 Gb/s Transceivers	8	8	16	24	16	28	32
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
Configuration	Configuration Memory (Mbits)	23.2	45.1	88.2	105.1	122.0	122.6	140.1
Package	Area	Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX Transceivers)						
Lidless flip chip BGA supporting 6.6 Gb/s serial line rates (1.0mm ball spacing)								
FBG484[4]	23 x 23 mm	185, 100 (4)	185, 100 (4)					
FBG676[4]	27 x 27 mm	200, 100 (8)	250, 150 (8)	250, 150 (8)		250, 150 (8)		
FBG900[4]	31 x 31 mm			350, 150 (16)		350, 150 (16)		
Flip chip BGA supporting 12.5 Gb/s serial line rates (1.0mm ball spacing)								
FFG676[4]	27 x 27 mm		250, 150 (8)	250, 150 (8)		250, 150 (8)		
FFG900[4]	31 x 31 mm			350, 150 (16)		350, 150 (16)		
FFG901[4]	31 x 31 mm				300, 0 (24)		350, 0 (28)	380, 0 (32)
FFG1156[4]	35 x 35 mm						350, 0 (28)	400, 0 (32)

6.6G

12.5G

Notes: 1. A single Kintex-7 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops, for a total of eight 6-LUTs and 16 Flip-Flops per CLB.
2. Refer to data sheet for details on I/O standards support.
3. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
4. Leaded package options ("FBxxx" or "FFxxx") available for the following Kintex-7 devices: XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, XC7K480T
5. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

From 4 to 32 GTX Transceivers @ up to 12.5G

Virtex-7T, XT and HT FPGAs

Virtex-7 FPGAs
Optimized for Highest System Performance and Capacity

											(1.0V)	
	Part Number		XC7V585T	XC7V2000T	XC7VX330T	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690T	XC7VX980T	XC7VX1140T	XC7VH580T	XC7VH870T
	EasyPath™ Cost Reduction Solutions[1]		XCE7V585T	XCE7V2000T	XCE7VX330T	XCE7VX415T	XCE7VX485T	XCE7VX550T	XCE7VX690T	XCE7VX980T	XCE7VX1140T	–	–
Logic Resources	Slices		91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000	90,700	136,900
	Logic Cells		582,720	1,954,560	326,400	412,160	485,760	554,240	693,120	979,200	1,139,200	580,480	876,160
	CLB Flip-Flops		728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000	725,600	1,095,200
Memory Resources	Maximum Distributed RAM (Kb)		6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700	8,850	13,275
	Block RAM/FIFO w/ ECC (36 Kb each)		795	1,292	750	880	1,030	1,180	1,470	1,500	1,880	940	1,410
	Total Block RAM (Kb)		28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680	33,840	50,760
Clocking	CMTs (1 MMCM + 1 PLL)		18	24	14	12	14	20	20	18	24	12	18
I/O Resources	Maximum Single-Ended I/O		850	1,200	700	600	700	600	1,000	900	1,100	600	650
	Maximum Differential I/O Pairs		408	576	336	288	336	288	480	432	528	288	312
Embedded IP Resources	DSP48E1 Slices		1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360	1,680	2,520
	PCI Express Gen2		3	4	—	—	4	—	—	—	—	—	—
	PCI Express Gen3		—	—	2	2	—	2	3	3	4	2	3
	Agile Mixed Signal (AMS) / XADC		1	1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1	1	1	1	1	1	1
	GTX 12.5 Gb/s Transceivers[2]		36	36	—	—	56	—	—	—	—	—	—
	GTH 13.1 Gb/s Transceivers[3]		—	—	28	48	—	80	80	72	96	48	72
	GTZ 28.05 Gb/s Transceivers		—	—	—	—	—	—	—	—	—	8	16
Speed Grades	Commercial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended[4]		-2L, -3	-2L, -2G	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L	-2L, -2G	-2L, -2G	-2L, -2G
	Industrial		-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1	—	—
	Package[5]	Area	Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX, GTH Transceivers)									1.8V SelectIO Pins (GTH, GTZ)	
	Flip chip, fine pitch BGA (1.0 mm ball spacing)												
	FFG1157	35 x 35 mm	0, 600 (20, 0)		0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (20, 0)		0, 600 (0, 20)				
Footprint Compatible	FFG1761	42.5 x 42.5 mm	100, 750 (36, 0)		50, 650 (0, 28)		0, 700 (28, 0)		0, 850 (0, 36)				
	FHG1761	45 x 45 mm		0, 850 (36, 0)									
	FLG1925	45 x 45 mm		0, 1200 (16, 0)									
	FFG1158	35 x 35 mm				0, 350 (0, 48)	0, 350 (48, 0)	0, 350 (0, 48)	0, 350 (0, 48)				
Footprint Compatible	FFG1926	45 x 45 mm							0, 720 (0, 64)	0, 720 (0, 64)			
	FLG1926	45 x 45 mm									0, 720 (0, 64)		
	FFG1927	45 x 45 mm				0, 600 (0, 48)	0, 600 (56, 0)	0, 600 (0, 80)	0, 600 (0, 80)				
Footprint Compatible	FFG1928	45 x 45 mm								0, 480 (0, 72)			
	FLG1928	45 x 45 mm									0, 480 (0, 96)		
Footprint Compatible	FFG1930	45 x 45 mm					0, 700 (24, 0)		0, 1000 (0, 24)	0, 900 (0, 24)			
	FLG1930	45 x 45 mm									0, 1100 (0, 24)		
	Ceramic flip chip, fine pitch BGA (1.0 mm ball spacing)												
	HCG1155	35 x 35 mm										400 (24, 8)	
	HCG1931	45 x 45 mm										600 (48, 8)	650 (48, 8)
	HCG1932	45 x 45 mm										300 (48, 8)	300 (72, 16)

From 16 to 96 Transceivers @ up to 13G+

Up to 16 Transceivers @ up to 28G

Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
2. 12.5 Gb/s support in "-3E", "-2GE" speed/temperature grade; 10.3125 Gb/s support in "2C", "-2LE", and "-2I" speed grade.
3. 13.1 Gb/s support in "-3E", "-2GE" speed grade; 11.3 Gb/s support in "2C" , "-2LE" and "-2I" speed/temperature grades.
4. -2G only applies to Stacked Silicon Interconnect devices and supports 12.5G GTX, 13.1G GTH, 28.05G GTZ with -2I fabric.
5. Leaded package options ("FFxxxx"/"FLxxxx"/"FHxxxx"/"HCxxxx") available for all packages.

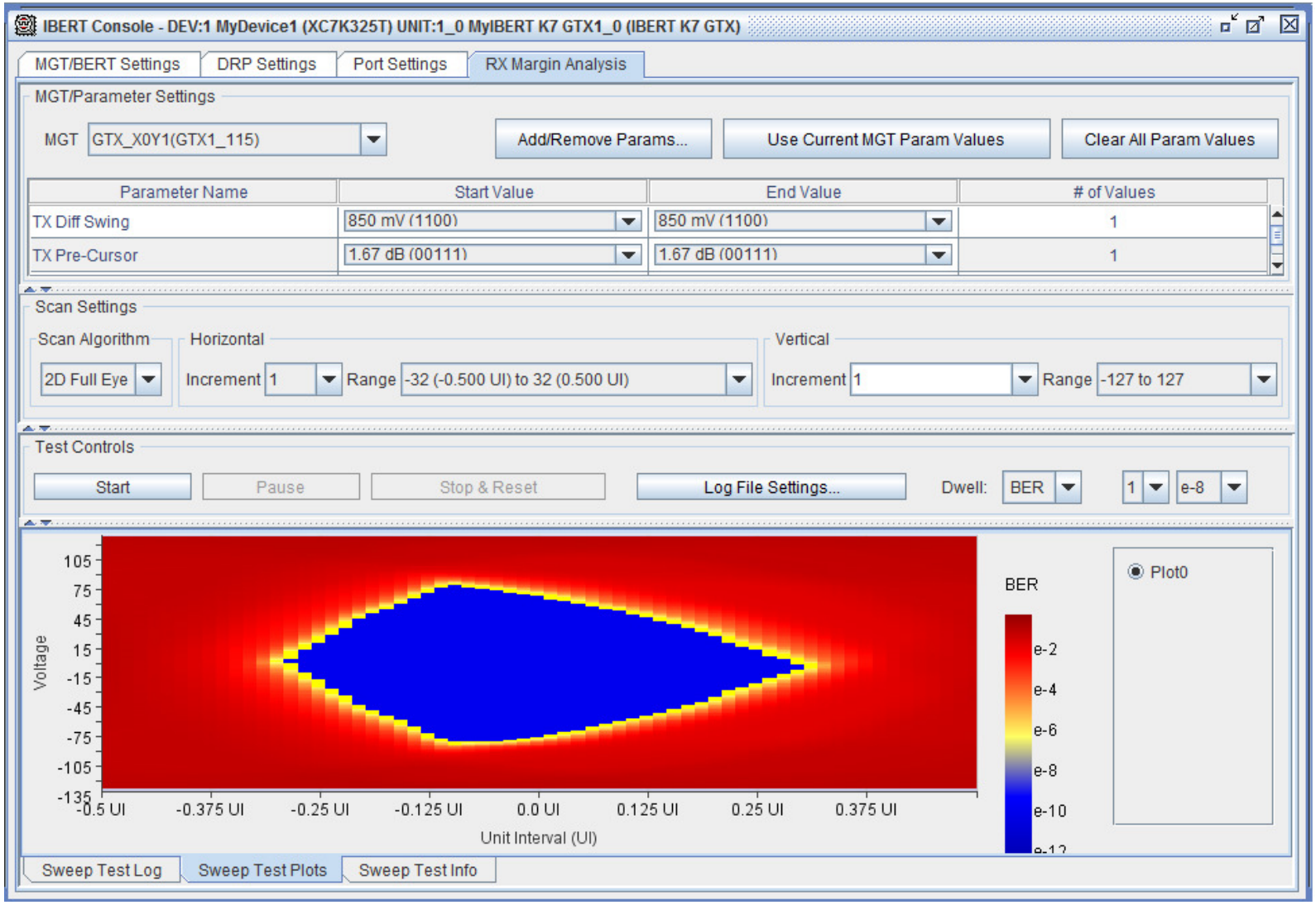
Summary

- **New for 7 Series:**
  - Common Transceiver Architecture
    - IP portability
  - Different Rates for different platforms
  - Low Power Mode
    - 30% lower power for chip-to-chip channels

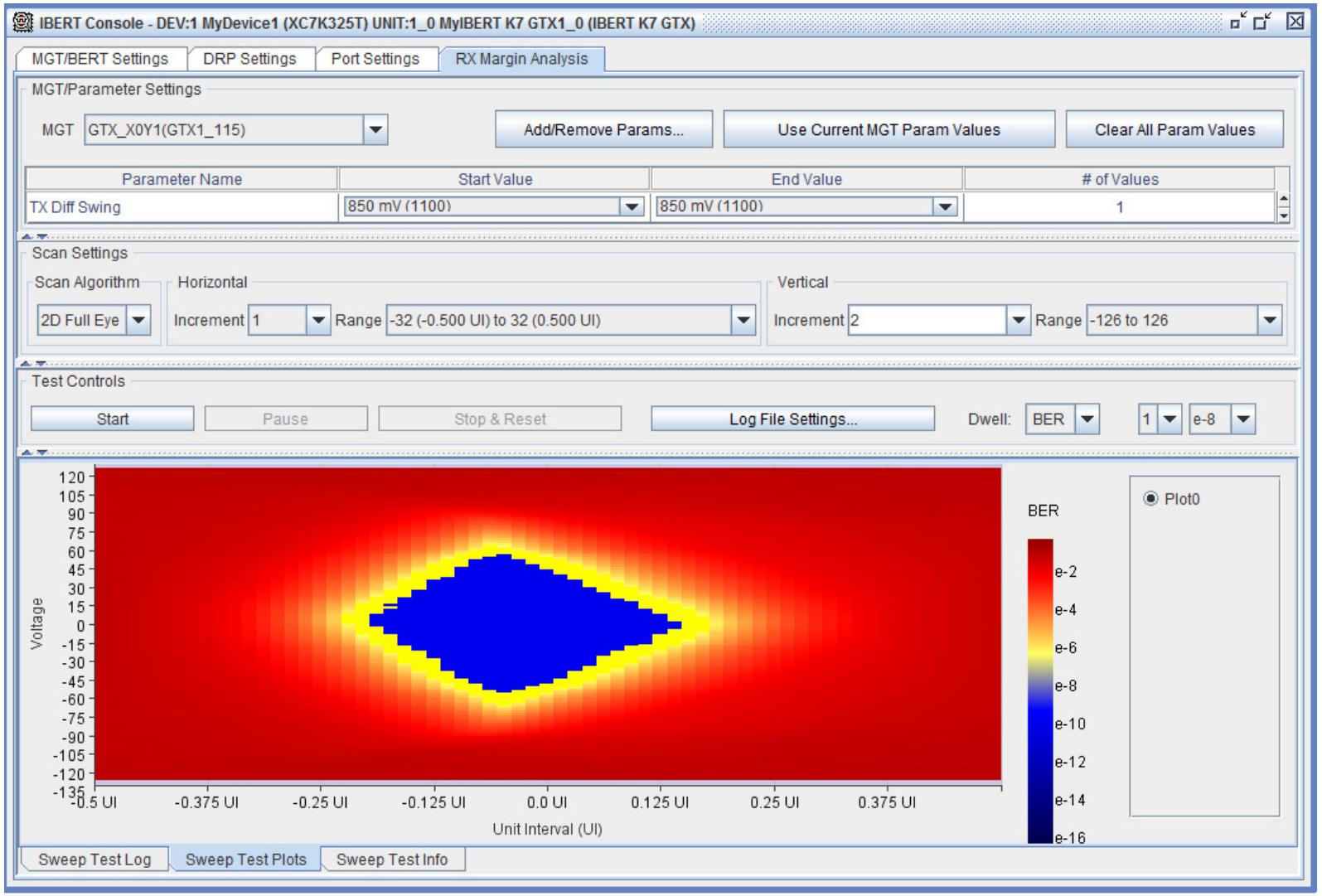
- **7 Series FPGAs Have the Most Comprehensive Transceiver Family**
  - Virtex-7 GTZ : 28Gb/s Transceivers for 100G and 400G datapaths
  - Virtex-7 GTH : Highest Performance/Count Transceiver Family
  - Virtex-7 GTX : 12.5Gb/s with more SelectIO for wider memory interfaces
  - Kintex-7 GTX : 12.5Gb/s to the masses
  - Artix-7 GTP : Ultra-High Volume Transceivers

Extra Slides

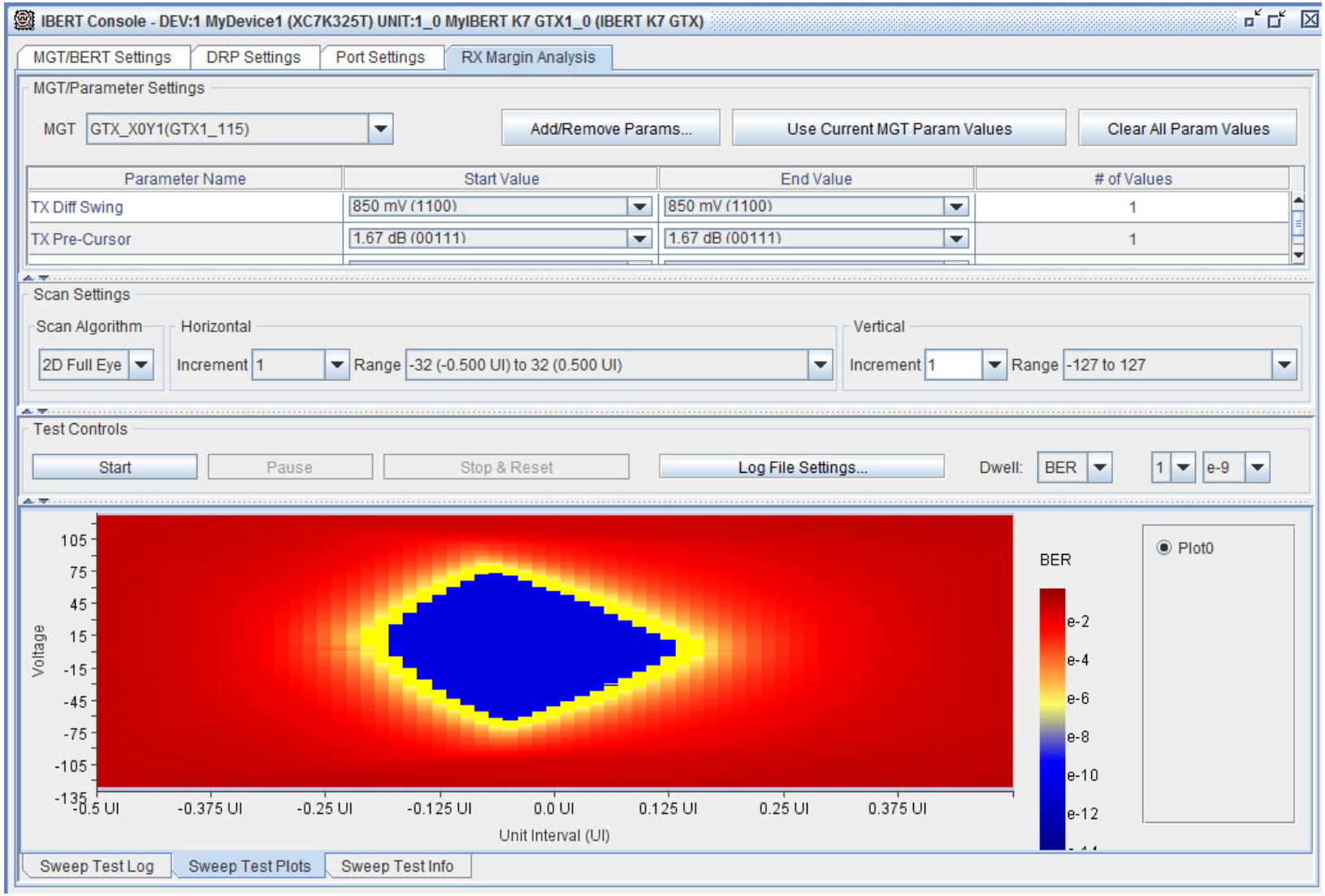
Scan Eye 12.5G 156.25MHz refclk (PRBS 7)



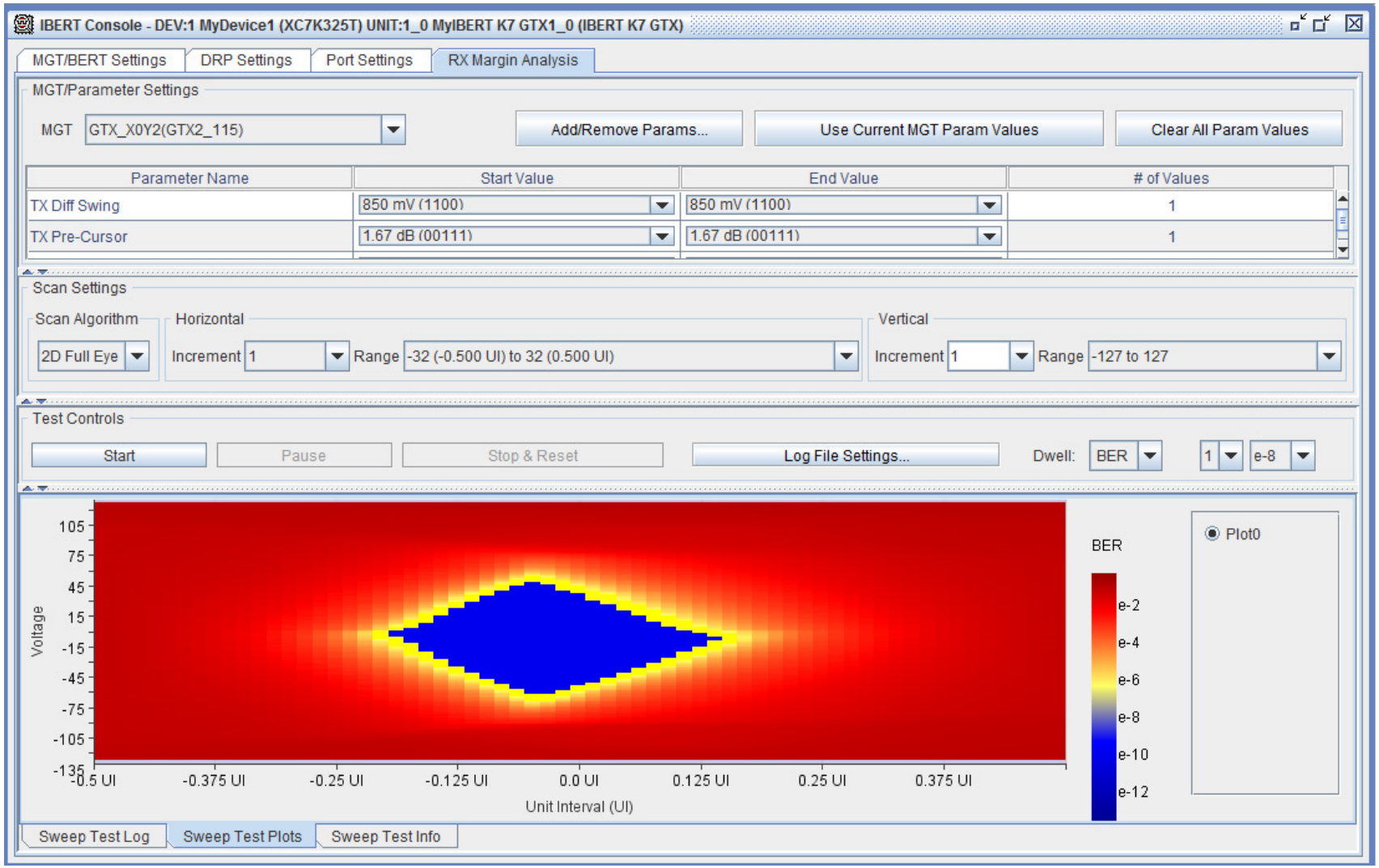
Scan Eye 12.5G 156.25MHz refclk (PRBS 31)



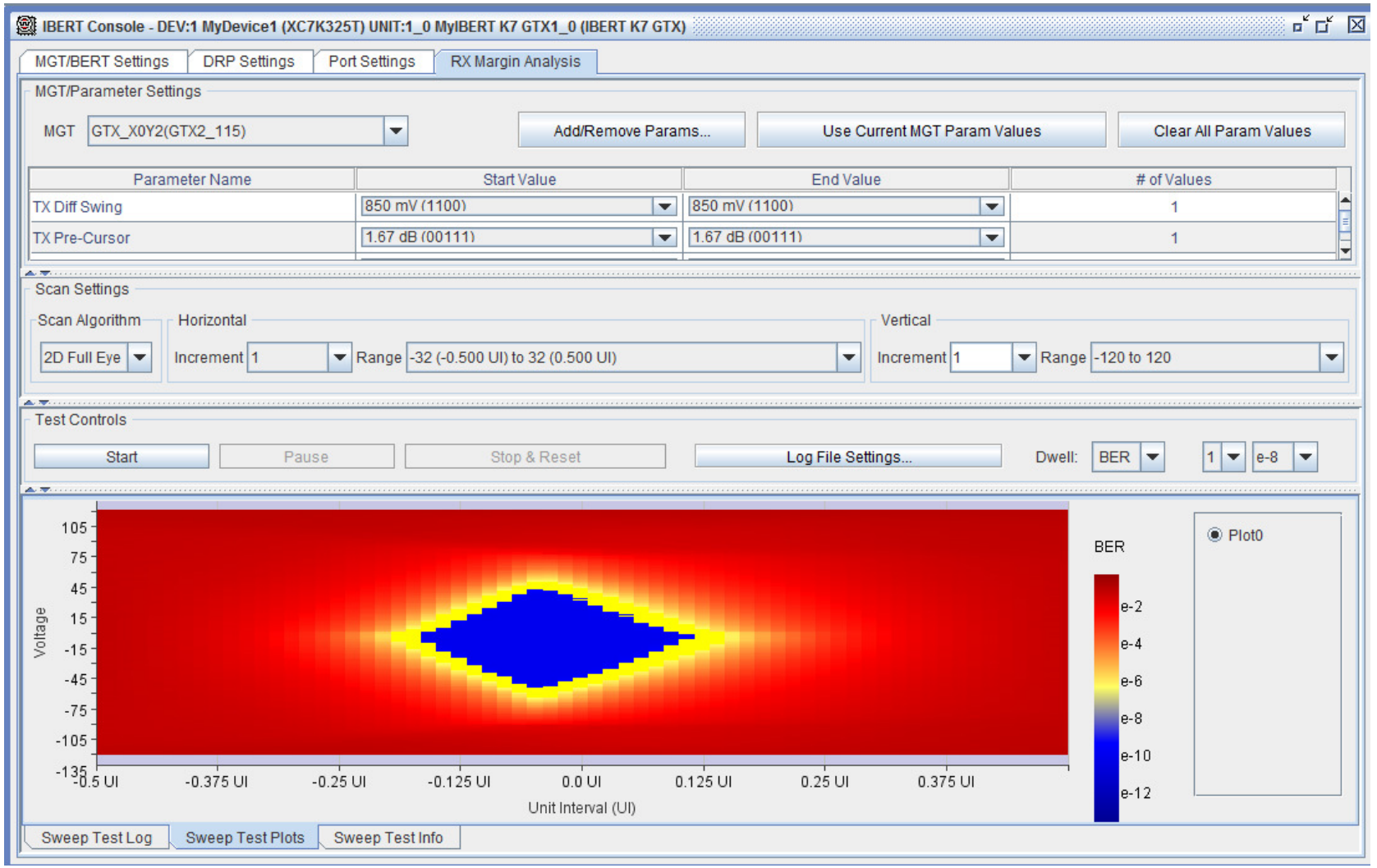
Scan Eye 10.3G 156Mhz refclk (PRBS 31)



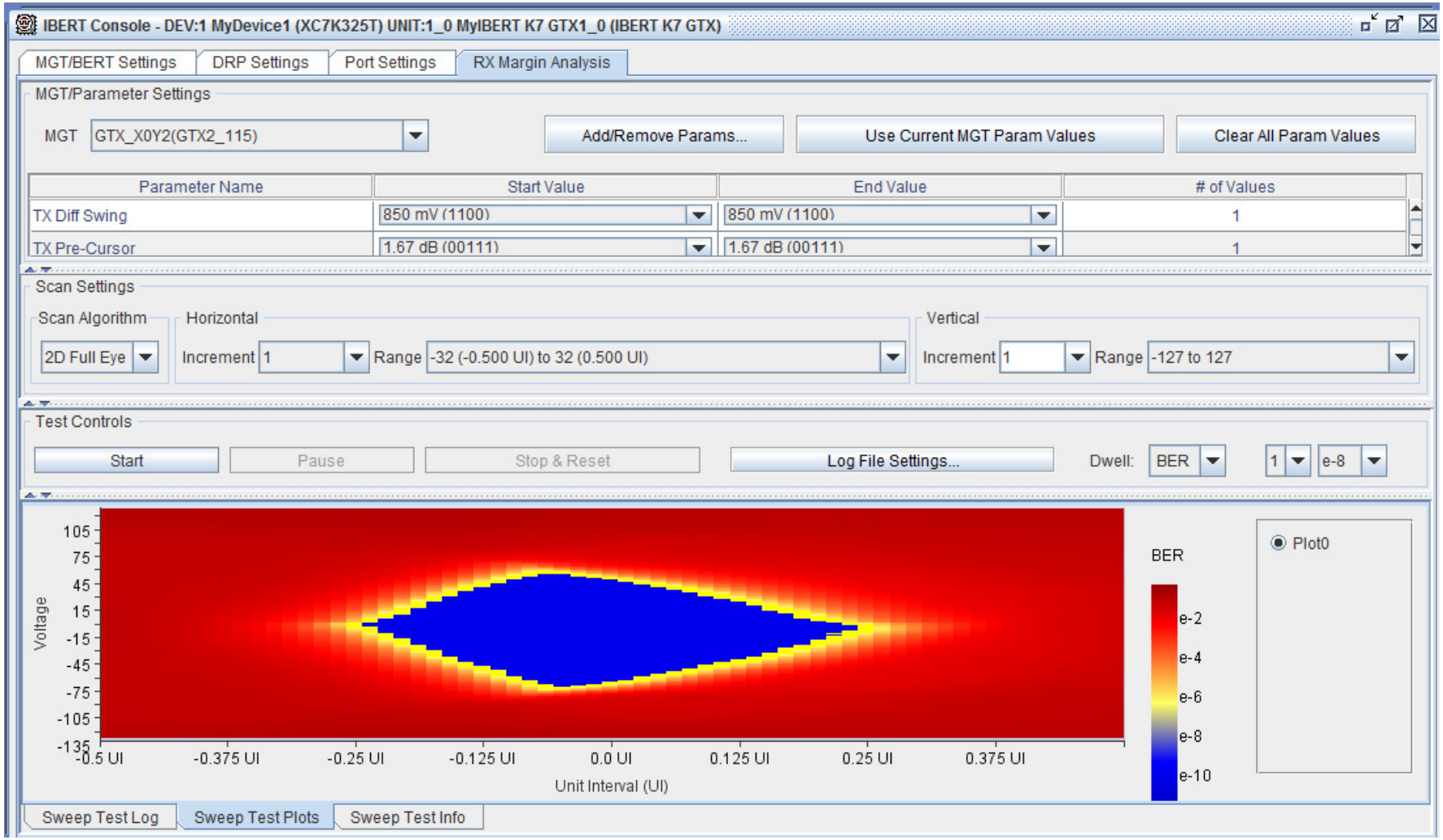
Scan Eye 10.3G 156.25MHz refclk (PRBS 7) Async



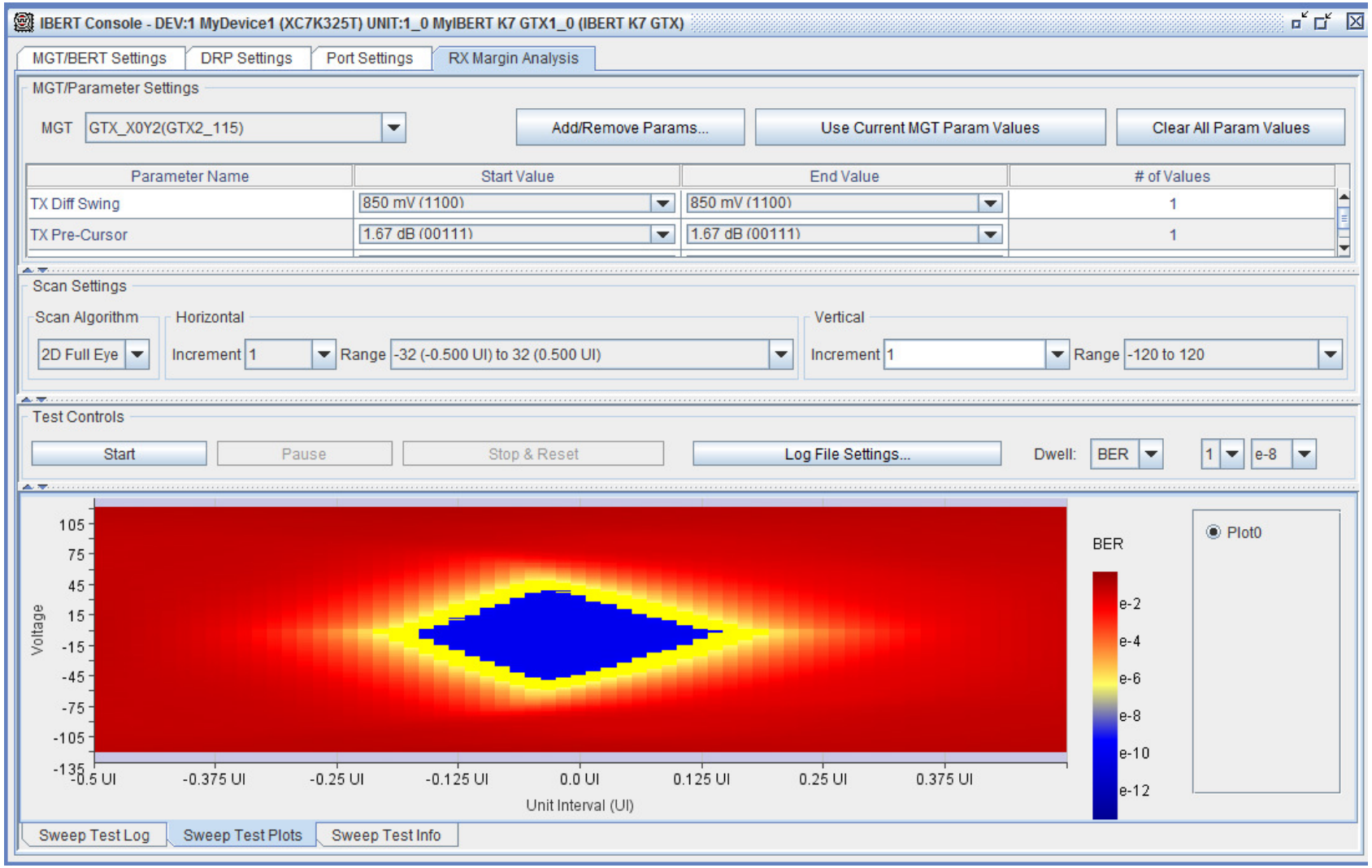
Scan Eye 10.3G 156.25MHz refclk (PRBS 31) Async



Scan Eye 12.5G 156.25MHz refclk (PRBS 7) Async



Scan Eye 12.5G 156.25MHz refclk (PRBS 31) Async



GTH Over Backplane @ 15.36Gbit/s

Paolo Novellini, System IO Specialist

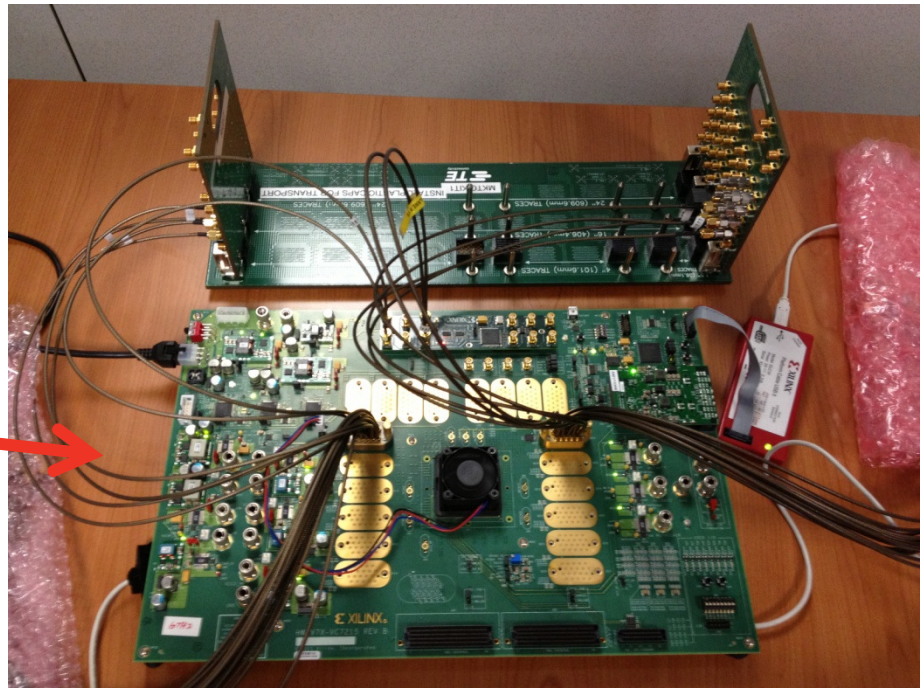
Agenda

- Introduction: purpose of presentation.
- Tyco Backplane description.
- 16 inches Tyco Backplane.
- 1 m Molex Backplane
- Conclusions.

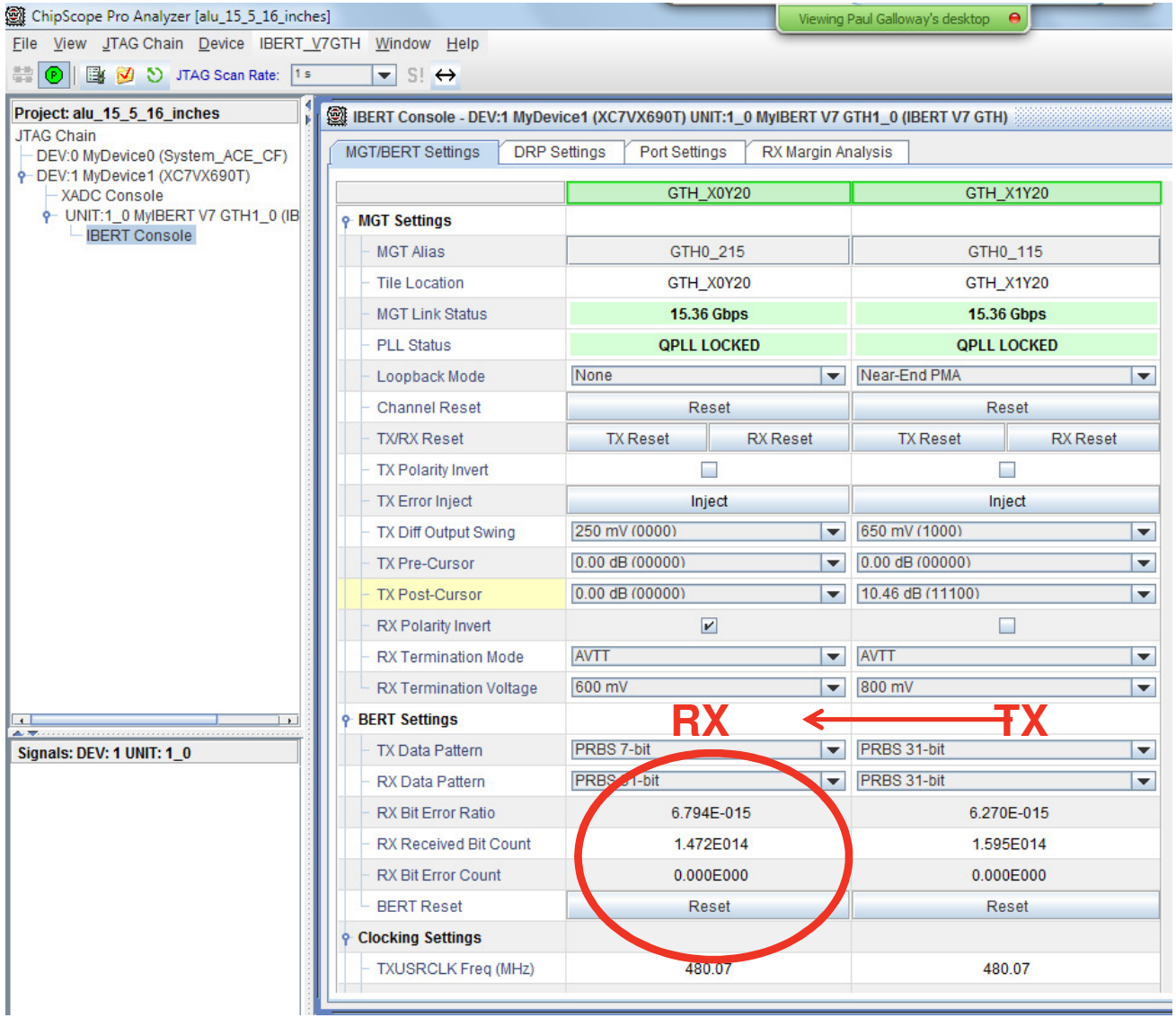
CASE 1

- **15.36 Gbit/s**
  - Prbs 31
  - 16 inches Tyco Backplane + 10 inches on the paddle cards

Virtex 7 on VC7215 Characterization Board



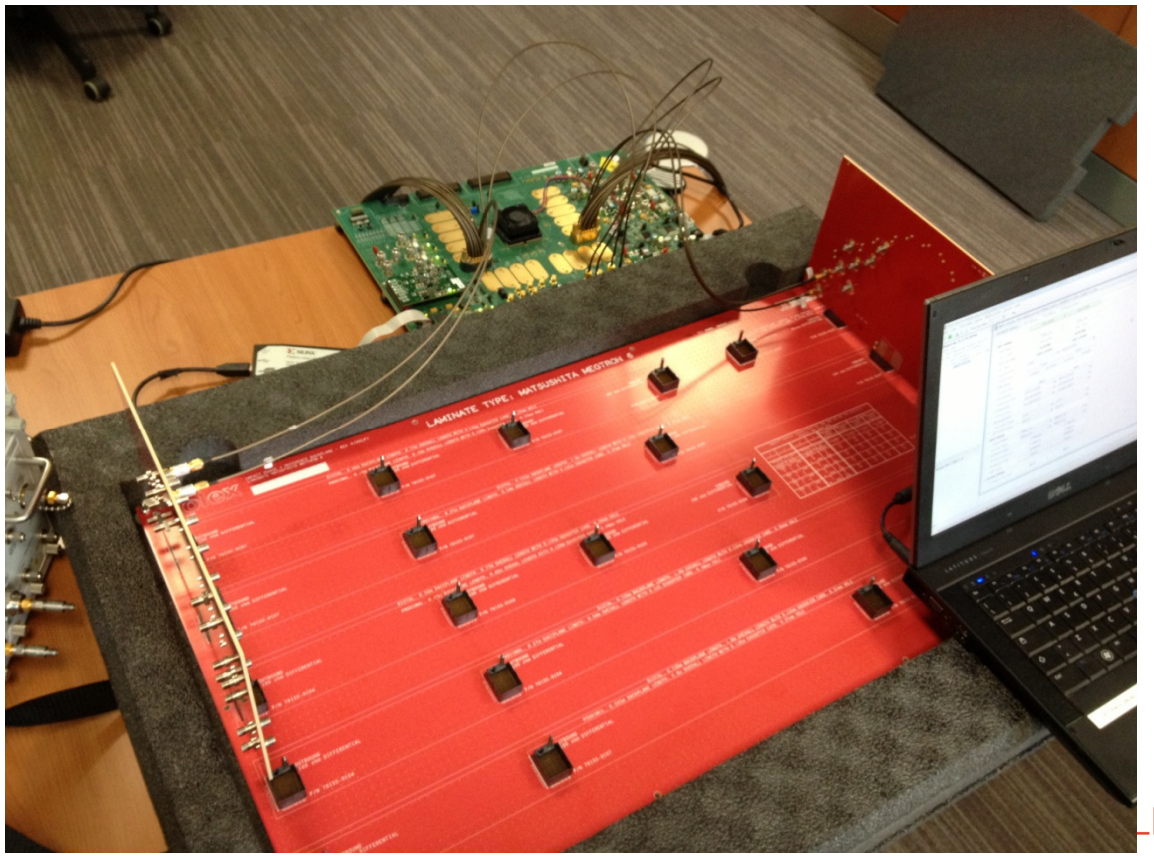
16 + 10 inches, 15.36G, BER<10-14, PRBS 31



CASE 2

15.36 Gbit/s

- Prbs 31
- 0.735 m MOLEX Backplane + 0.27 m on the paddle cards: 1 meter

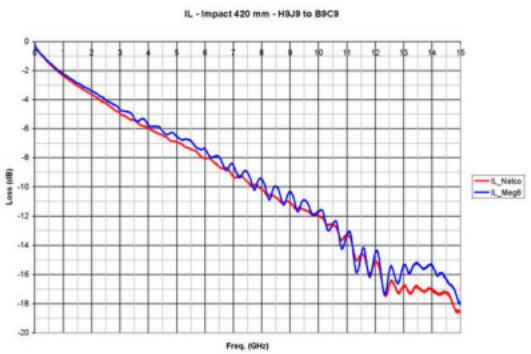


Molex BACKPLANE – IMPACT Connector

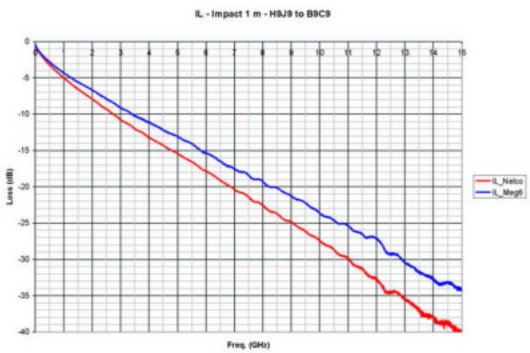
- http://www.molex.com/mx_upload/family/gbx_itrac_backplane_connector_system/ImpactKRchannelmeasuredanalysis.pdf

PCB Material Insertion Loss

420mm (16.5") Channel



1m (39.4") Channel

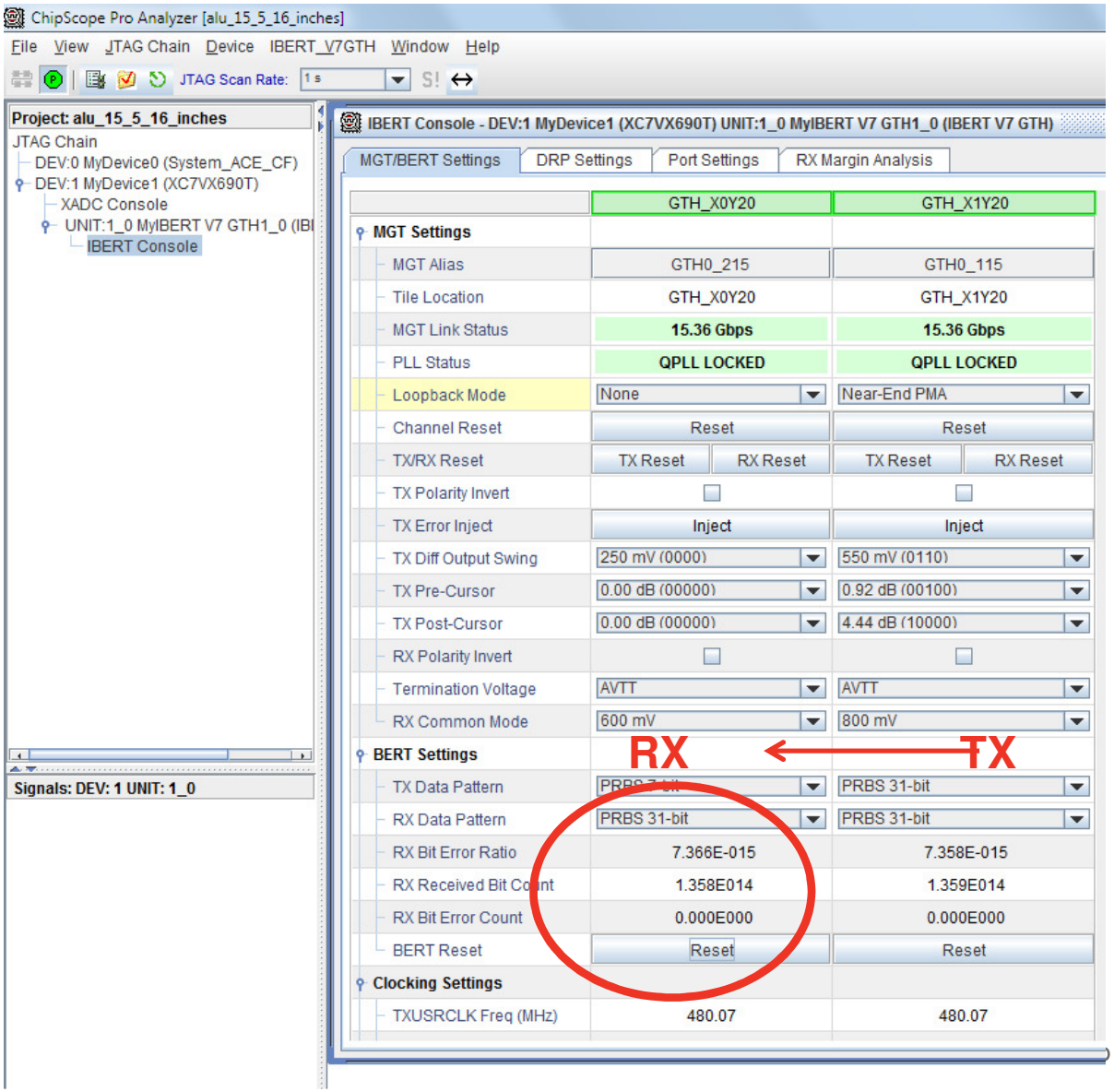


Legend

- Nelco4000-13SI VLP Finish
- Megtron 6 HVLP Finish

20 db@8GHz!!

1 m, 15.36G, BER<10-14, PRBS 31



Remarks

- **GTH runs at room temperature at 15.36G in a stable way down to 10-14**
- **PRBS 31**
- **16 inches of Nelco FR4, with 2 paddle cards and 2 TYCO Z-PACK connectors.**
  - Each paddle card is 5 inches
- **0.73 m of Megtron 6, with 2 paddle cards and 2 Molex Impact**
  - Each paddle cards add 0.13 m
- **15.5G over backplane is next gen silicon is low risk.**