Zynq EPP Architecture

Objectives

- What is the Zynq Extensible Processing Platform
- Comparison of Xilinx Processing Solutions
- Programmable logic (PL) differences to other FPGAs
- Simulation and debugging

What is the Zynq Extensible Processing Platform (EPP)?

- **Not an ordinary FPGA!**
- **Not an ordinary microprocessor!**
- **Unique blend of the two technologies**
  - Dual ARM Cortex™-A9 processors + caches + robust peripheral set
  - 7 series fabric
  - Plus powerful interconnects between the two
- ***It's no longer just an FPGA, it's a processing system with programmable logic!***

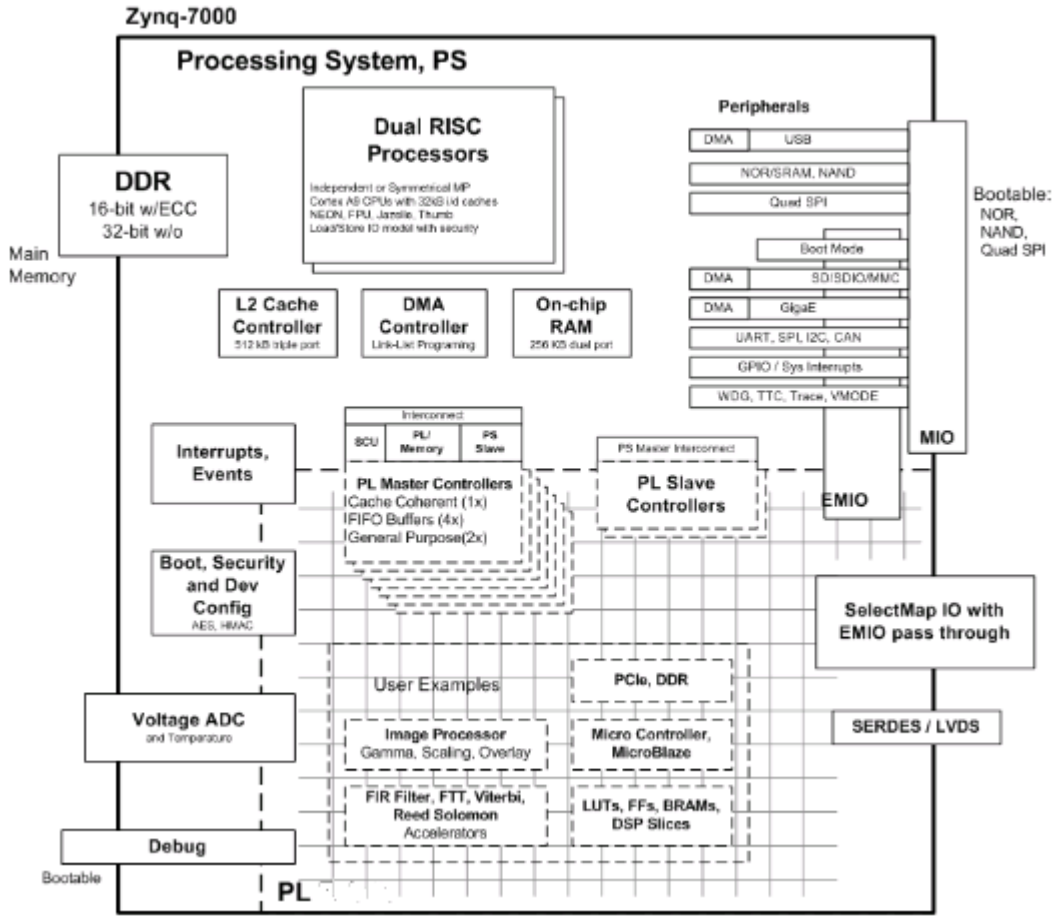
Devices

Zynq-7000 All Programmable SoC					
	Device Name	**Z-7010**	**Z-7020**	**Z-7030**	**Z-7045**
	Part Number	**XC7Z010**	**XC7Z020**	**XC7Z030**	**XC7Z045**
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA	Artix-7 FPGA	Kintex™-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates (3)	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	350K Logic Cells (~5.2M)
	Look-Up Tables (LUTs)	17,600	53,200	78,600	218,600
	Flip-Flops	35,200	106,400	157,200	437,200
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	560 KB (140)	1,060 KB (265)	2,180 KB (545)
	Programmable DSP Slices (18x25 MACCs)	80	220	400	900
	Peak DSP Performance (Symmetric FIR)	100 GMACs	276 GMACs	593 GMACs	1,334 GMACs
	PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8
	Agile Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs			
	Security (2)	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication			

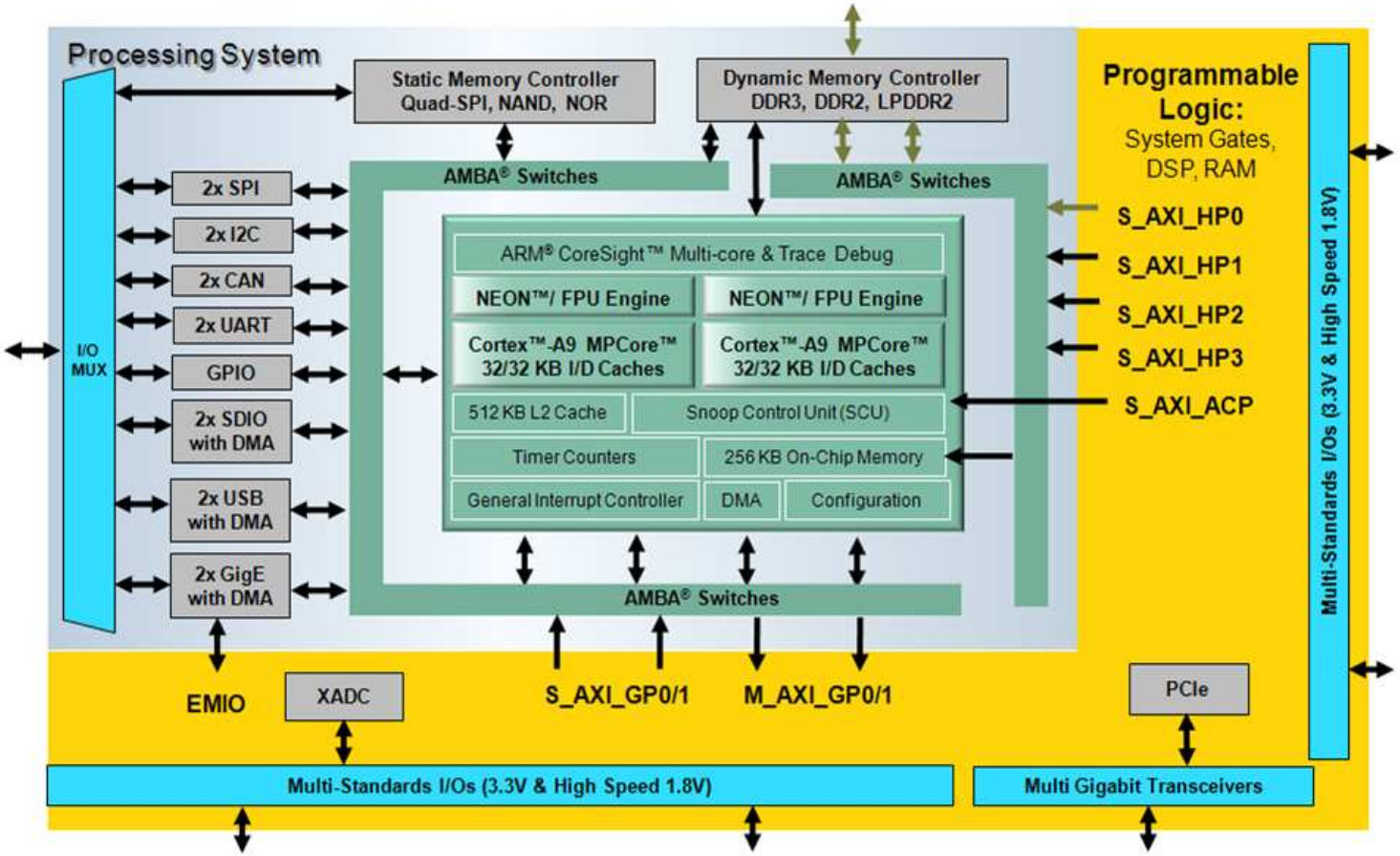
Notes:

1. Restrictions apply for CLG225 package. Refer to the UG585, *Zynq-7000 EPP Technical Reference Manual* (TRM) for details.
2. Security is shared by the Processing System and the Programmable Logic.
3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

Zynq EPP PS and PL Block Diagram



Zynq-7000 EPP Block Diagram



PS-PL Bandwidth

- S_AXI_HPx: 4If * 8Byte * 150MHz = 4800MB Rd + 4800MB Wr
- S_AXI_ACP: 8Byte * 150MHz[1] = 1200MB Rd + 1200MB Wr
- S_AXI_GPx: 2If * 4Byte * 150MHz = 1200MB Rd + 1200MB Wr
- M_AXI_GPx: 2If * 4Byte * 150MHz = 1200MB Rd + 1200MB Wr

- DDR3: 1066Mb/s * 32Pins = 4264MB/s
  1333Mb/s * 32Pins = 5332MB/s

- NOR/SRAM: 125MHz * 8Bit = 125MB/s
- NAND: 50MHz * 16Bit = 100MB/s
- QSPI: 100MHz * 4Bit = 50MB/s
- SDIO: 50MHz * 4Bit = 25MB/s

[1] not defined in DS187 1.2, DS191 1.1

Comparison of Xilinx Processing Solutions

PowerPC 405

- **Available in Virtex-II Pro (2002) and Virtex-4 (2004)**
- **Performance: 1.56DMIPS/MHz, 400MHz**
- **Architecture:**
  - 1st level cache: 16kB + 16kB, 2-way set-associative
  - 5 stage pipeline
  - 32 registers
- **Peripherals: 3 processor timer**
- **Programming: powerpc-eabi-gcc 4.1.1**
- **Infos: PowerPC 405 Processor Block Reference Guide UG018**

PowerPC 440

- **Available in Virtex-5 (2006)**
- **Performance: 2DMIPS/MHz, 550MHz**
- **Architecture:**
  - 1st level cache: 32kB + 32kB, 64-way set-associative
  - 7 stage pipeline, 3 execution pipelines
  - 32 registers
- **Peripherals:**
  - 3 processor timer
  - crossbar with 3 PLB and 4 DMA (LocalLink) interfaces
- **Programming: powerpc-eabi-gcc 4.1.1**
- **Infos: Embedded Processor Block in Virtex-5 FPGAs Reference Guide UG200**

ARM Cortex-A9

- **Available in Zynq-7000 (2012)**
- **Performance: 2.5DMIPS/MHz, 1000MHz**
- **Architecture:**
  - 1st level cache: 32kB + 32kB, 4-way set-associative
  - 512kB shared unified L2 cache, 8-way set-associative
  - 8 stage pipeline, 4 execution pipelines
  - 16 registers
- **Peripherals:**
  - NEON vector processing unit and VFP3 FPU
  - Snoop control unit (SCU) with Accelerator Coherency Port (ACP)
  - General interrupt controller (GIC)
  - On-chip memory (OCM): 256kB RAM and (hidden) boot ROM
  - Central DMA with 8 channels
  - Private timer and watchdog timer for each CPU
  - System watchdog and two triple timer counters shared between CPUs

- **Peripherals (continued):**
  - Device configuration (DEVCFG) with DMA for PL read and write (100MB/s secure, 400MB/s unsecure)
  - DDR3/2 memory controller
  - NAND/NOR/SRAM/QSPI memory controller
  - Two USB 2.0 OTG, two tri-mode gigabit Ethernet
  - Two SDIO, CAN 2.0Bs, SPIs, I2Cs, UARTs
  - four GPIO 32-bit blocks
  - two high performance AXI interconnects and 9 AXI interfaces to PL
- **Programming:**
  - arm-xilinx-eabi-gcc 4.6.1
  - arm-xilinx-linux-eabi-gcc 4.6.1
- **Infos: Zynq-7000 Technical Reference Manual UG585[2]**

[2] ~1700 pages

MicroBlaze v8.40

- **Softcore available in all Xilinx FPGAs (2002)**
- **Performance:**
  - 1.03DMIPS/MHz, 300MHz (area optimized)
  - 1.38DMIPS/MHz, 247MHz (performance optimized)
- **Architecture:**
  - 1st level cache: 0,64B-64kB + 0,64B-64kB, direct mapped
  - Victim cache and system cache
  - 3 stage pipeline (area optimized), 5 stage pipeline (performance optimized)
  - 32 registers
- **Peripherals: none**
- **Programming: mb-gcc 4.6.2**
- **Special Features:**
  - Lockstep support
  - fault tolerant features
  - low latency interrupt mode

MicroBlaze v8.40

- **Resources:**
  - MicroBlaze with minimum area and 32kB RAM (incl MDM, reset module, clock generator, GPIO, timer) =
    =8BRAMs, 1709Regs, 1603LUTs ~ 10% Z-7010
  - MicroBlaze with maximum performance (4kB + 4kB cache) and 32kB RAM (incl MDM, reset module, clock generator, DDR3, I2C, 6 UART, 4 SPI, interrupt controller, timer, ethernet controller, BRAM-interface) =
    =17BRAMs, 9006Regs, 11028LUTs ~ 40% Z-7010

- **Infos: MicroBlaze Processor Reference Guide UG081**

PicoBlaze

- **Softcore available in all Xilinx FPGAs, CPLDs (2000)**
- **Performance: 0.5MIPS/MHz, 240MHz**
- **Architecture:**
  - 8-bit RISC
  - 64 bytes scratchpad RAM
  - 2*16 registers
- **Peripherals: 256 input and 256 output ports**
- **Programming: assembler**
- **Special Features:**
  - 2 cycles per instruction
  - worst case interrupt latency = 5 cycles
- **Resources:**
  - 1BRAMs, 26 Slices (=) ~ 0.6% Z-7010
- **Infos: PicoBlaze User Guide UG129**

Real World Comparison lwIP iperf

- **MicroBlaze 75MHz, 32kB cache, EthernetLite, SP605, XilKernel**
  - Raw mode: RX=52Mb/s, TX=35Mb/s
  - Socket mode: RX=22Mb/s, TX=24Mb/s
- **MicroBlaze 100MHz, 32kB cache, Ethernet (DMA), ML605, XilKernel**
  - Raw mode: RX=204Mb/s, TX=170Mb/s
  - Socket mode: RX=42Mb/s, TX=37Mb/s
- **PowerPC 440 400MHz, ML507, XilKernel**
  - Raw mode: RX=500Mb/s, TX=440Mb/s
  - Socket mode: RX=160Mb/s, TX=240Mb/s
- **ARM Cortex-A9 666MHz, ZC702, FreeRTOS**
  - Raw mode: RX=943Mb/s, TX=810Mb/s
  - Socket mode: RX=490Mb/s, TX=550Mb/s
- **Infos: LightWeight IP (lwIP) Appl. Ex. XAPP1026 (since 2008)**

Programmable Logic

Programmable Logic (PL)

- **7 series programmable logic**
  - Artix™ device based: Z-7010 and Z-7020
    - HR I/O blocks
  - Kintex™ device based: Z-7030 and Z-7045
    - HR and HP I/O blocks
    - GTx up to 12.5Gbps
    - PCIe core Gen2, 8 lanes
    - Xilinx Analog Mixed Signal (AMS) system: 1Msps,12-bit dual converter XADC with up to 17 input channels
- **Software configurable after processor boot via the PL device configuration module (100MB/s secure, 400MB/s unsecure)**
- **Independent of the PS**
  - Separate on-chip power planes
  - Clock and reset management

PL-PS AXI Interfaces

- **AXI high-performance slave ports (HP0-HP3)**
  - Configurable 32-bit or 64-bit data width
  - Access to OCM and DDR only
  - Conversion to processing system clock domain
  - AXI FIFO Interface (AFI) are FIFOs (1KB) to smooth large data transfers
- **AXI general-purpose ports (GP0-GP1, GP2-GP3)**
  - Two masters from PS to PL
  - Two slaves from PL to PS
  - 32-bit data width
  - Conversation and sync to processing system clock domain
- **One 64-bit accelerator coherence port (ACP) AXI slave interface to CPU memory**

PL-PS Interfaces

- **DMA, interrupts, events signals**
  - Processor event bus for signaling event information to the CPU
  - PL peripheral IP interrupts (16+4) to the PS general interrupt controller (GIC)
  - Four DMA channel RDY/VALID/TYPE signals
- **Extended multiplexed I/O (EMIO) allows PS peripheral ports access to PL logic and device I/O pins**
- **Clock and resets**
  - Four PS clock outputs to the PL with enable control
  - Four PS reset outputs to the PL
- **Configuration and miscellaneous**
  - Idle AXI to PS

PS Boots First

- **CPU0 boots from OCM ROM; CPU1 goes into a sleep state**
- **On-chip boot loader in OCM ROM (Stage 0 boot)**
- **Processor loads First Stage Boot Loader (FSBL) from external flash memory selected via bootstrapping pins**
  - NOR (40 Pins MIO, 64MB)
  - NAND (15 or 23 Pins MIO for 8,16-bit memory; ~1GB)
  - Quad-SPI (8,9 or 14 Pins MIO, 16 or 32MB)
  - SD Card (6 Pins MIO, FAT32 file system reading boot.bin)
  - JTAG; not a memory device—used for development/debug only
- **Optional secure boot mode allows the loading of encrypted software from the flash boot memory**
- **The programmable logic is configured after the PS boots by application software accessing the hardware device configuration unit**
  - Bitstream image transferred with 100-MHz, 32-bit PCAP stream interface
  - Decryption/authentication hardware option for encrypted bitstreams
  - In secure boot mode, this option can be used for software memory load
  - Built-in DMA allows simultaneous PL configuration and OS memory loading

Simulation and debugging

Hardware

- **Avoid debugging**
  - Add AXI interface to your design with Create or/and Import Peripheral Wizard
- **Verify with AXI Bus Functional Models developed by Cadence**
  - Sequence of Verilog tasks contained in a Verilog-syntax text file
- **The Zynq EPP extensible virtual platform from Cadence**
  - A fast instruction set simulator for the ARM Cortex-A9 MPCore processor
  - Models register interface for all Zynq-7000 devices
  - Models function of key Zynq-7000 EPP and on-board devices
  - Extensible using TLM (C or SystemC models)
    - Peripherals, accelerators, and any other IP in the programmable logic or on the board
- **Chipscope with AXI Bus Monitor, AXI Performance Monitor, ILA and VIO**
  - Cross trigger with CoreSight in the PS (Hardware event forces a program breakpoint, Software breakpoint triggers logic analyzer)

Hardware in the Loop (HIL) Simulation

- All AXI IPs are simulated in ISim (clocked by the testbench clock)
- PS is simulated in Hardware (free running mode)
- Connected with JTAG
- Advantages:
  - Simulation speed
  - Cycle-accurate simulation of the PL
  - Quick design turns for HW and SW
- Limitations:
  - Only AXI connections between PS and PL
  - Only one testbench clock
  - No interrupt support
  - Design has to be modified to bring out clock and reset

Software

- **The Zynq EPP extensible virtual platform from Cadence**
- **QEMU simulation**
  - System and OS (Linux) emulation
- **ARM CoreSight architecture**
  - Embedded trace buffer (ETB), Program trace module (PTM), Instrument trace module (ITM)
  - Xilinx adds AXI monitor (AXIM) and Fabric trace module (FTM)
  - Software debug with SDK
  - Third-party tools via their cables!!!

References

- **Xilinx Trainings**
  - How to Design Xilinx Embedded Systems in 1 Day
  - Essentials of Microprocessors
  - Introduction to the Zynq All Programmable SoC Architecture
  - Zynq All Programmable SoC System Architecture
  - Embedded Linux
  - Embedded Systems Development
  - Advanced Features and Techniques of Embedded Systems Development
  - Embeded Systems Software Development
  - Advanced Features and Techniques of Embedded Systems Software Design
  - C Language Programming with SDK

- Zynq-7000 All Programmable SoC Technical Reference Manual UG585
- Master Answer Record http://www.xilinx.com/support/answers/47916.htm
- Hardware In The Loop (HIL) Simulation for the Zynq-7000 All Programmable SoC XAPP744
- Xilinx User Community Forums http://forums.xilinx.com/
- ARM documentation http://infocenter.arm.com/help/index.jsp
- ARM forums http://forums.arm.com/

- Zynq-7000 All Programmable SoC Software Developers Guide UG821
- ARM® Architecture Reference Manual ARMv7-A and ARMv7-R edition DDI0406C_arm_architecture_reference_manual.pdf[3]
- Open Source Linux http://wiki.xilinx.com/zynq-linux
- Zynq U-boot boot loader http://wiki.xilinx.com/zynq-uboot
- QEMU for Zynq http://wiki.xilinx.com/zynq-qemu

[3] 2680 pages